88F5182

Feroceon® Storage Networking SoC

Datasheet

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Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.x

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PRODUCT OVERVIEW

The Marvell® 88F5182 device is a high-performance, highly integrated, Storage Networking System Engine. It is based on the Marvell Feroceon® CPU core, which is fully compliant with the ARMv5TE.

FEATURES

- **High-performance integrated controller**
  - High-performance Feroceon CPU core with integrated 32/32 KB I/D L1 cache, running at up to 500 MHz
  - High bandwidth dual-port memory controller (16-/32-bit DDR1/DDR2 SDRAM)
  - Single PCI Express (x1) port with integrated PHY
  - Single 32-bit PCI2.2 66 MHz port
  - Two SATA 2.0 ports with integrated 3 Gbps SATA II PHYs
  - Single Gigabit Ethernet MAC (10/100/1000 Mbps)
  - Two USB 2.0 ports with integrated PHY
  - Security Cryptographic Engine
  - Two-Wire Serial Interface (TWSI)
  - Two UART ports
  - 16-bit device bus with up to four chip selects
  - NAND Flash Support
  - Integrated DMA engine (four channels)
  - XOR engine for RAID applications
  - 26 multi-purpose pins
  - Interrupt controller
  - Timers
- **Marvell® Feroceon® CPU core**
  - 500 MHz with DDR1/DDR2 at 166 MHz
  - 400 MHz with DDR2 at 200 MHz
  - 32-bit and 16-bit RISC architecture
  - Compliant with v5TE architecture as published in the ARM Architect Reference Manual, Second Edition
  - Includes MMU to support virtual memory features
  - MPU can be used instead when not using MMU
  - 32-KB I-Cache and 32-KB D-Cache
  - 64-bit internal data bus
  - Out-of-order execution for increased performance
  - In-order retire via a Reordering Buffer (ROB)
  - Branch Prediction Unit
  - Supports JTAG/ARM Multi-ICE
  - Supports both Big and Little Endian modes
- **DDR1/DDR2 SDRAM controller**
  - DDR SDRAM with a clock ratio of 1:1, 1:2, 1:3, or 1:4 between the DDR SDRAM and the Feroceon CPU core, respectively
  - 16-/32-bit interface
  - DDR1 at up to 333 MHz
  - DDR2 at up to 400 MHz
  - Supports up to two dual-sided DIMMs
  - Supports DDR components of x8 and x16
  - Dual channel memory controller
  - Reduced CPU to DDR SDRAM latency
  - SSTL 2.5V I/Os in DDR1, 1.8V I/Os in DDR2
  - Supports four DDR SDRAM banks (CSs)
  - DDR1 supports device densities of 128, 256, 512 Mbits
  - DDR2 supports device densities of 256, 512 Mbits
  - Up to 1 GB (32-bit interface) and 0.5 GB (16-bit interface) total memory space
  - Supports DDR SDRAM bank interleaving between all DDR SDRAM banks (both the physical banks, and the four internal banks of the DDR SDRAM devices)
  - Supports up to 16 open pages (page per bank)
  - Supports configurable DDR SDRAM timing parameters
  - Supports up to 32-byte burst per single DDR SDRAM access
  - Single ended DQS in DDR2
  - DDR1/DDR2 pad auto calibration
  - Support DDR2 On Die Termination (ODT)
- **PCI Express interface (x1)**
  - PCI Express Base 1.0a compatible
  - Integrated low power SERDES PHY, based on proven Marvell SERDES technology
  - Root Complex port
  - Can be configured also as an Endpoint port
  - x1 link width

- 2.5 GHz/s signalling
- Lane polarity reversal support
- Maximum payload size of 128 bytes
- Single Virtual Channel (VC-0)
- Replay buffer support
- Extended PCI Express configuration space
- Advanced Error Reporting (AER) support
- Power management: L0s and software L1 support
- Interrupt emulation message support
- Error message support

■ **PCI Express master specific features**
- Single outstanding read transaction
- Maximum read request of up to 128 bytes
- Maximum write request of up to 128 bytes
- Up to four outstanding read transactions in Endpoint mode

■ **PCI Express target specific features**
- Supports up to eight read request transactions
- Maximum read request size of 4 KB
- Maximum write request of 128 bytes
- Supports PCI Express access to all of the device's internal registers

■ **32-bit PCI interface**
- 66 MHz PCI 2.2 compliant interface
- 3.3V I/Os, 5V tolerant
- Supports 64-bit addressing via DAC transactions
- Configurable PCI arbiter for up to six masters

■ **PCI master specific features**
- Supports all PCI cycles
- Host to PCI bridge—translates CPU cycles to PCI memory, I/O, or configuration cycles
- Supports DMA bursts between PCI and memory
- Supports transaction combining to unlimited PCI burst

■ **PCI target specific features**
- Supports all PCI cycles
- Supports programmable aggressive read prefetch
- Supports unlimited burst write with zero wait states
- Supports up to four delayed reads
- Supports PCI access to all of the device's internal registers
- PCI address remapping to local memory

■ **PICMG Compact PCI Hot-Swap ready**

■ **PCI "Plug and Play" support**
- Plug and Play compatible configuration registers
- PCI configuration registers that are accessible from both the Feroceon CPU core and PCI
- Vital Product Data (VPD) support
- PCI Power Management (PMG) support
- Message Signal Interrupts (MSI) support

■ **SATA II interface (2 ports)**
- Integrates Marvell 3 Gbps (Gen2i) SATA PHY
- Compliant with SATA II Phase 1 specifications
  - Supports SATA II Native Command Queuing (NCQ), up to 128 outstanding commands per port
  - First party DMA (FPDMA) full support
  - Backwards compatible with SATA I devices
- Supports SATA II Phase 2 advanced features
  - 3 Gbps (Gen2i) SATA II speed
  - Port Multiplier (PM)—Performs FIS-Based Switching as defined in SATA working group PM definition
  - Port Selector (PS)—Issues the protocol-based OOB sequence to select the active host port
- Supports device 48-bit addressing
- Supports ATA Tag Command Queuing

■ **SATA II Host Controller**
- Enhanced-DMA [EDMA] per SATA port
  - Automatic command execution without host intervention
  - Command queuing support, for up to 128 outstanding commands
  - Separate SATA request/response queues
  - 64-bit addressing support for descriptors and data buffers in system memory
- Read ahead
- Advanced interrupt coalescing
- Target mode operation—Two 88F5182 devices can be attached through Serial-ATA ports, enabling data communication between different 88F5182 devices.
- Advanced drive diagnostics via the ATA SMART command

■ **Integrated single GbE (10/100/1000) MAC**
- Supports 10/100/1000 Mbps
- MII, GMII, or RGMII Interface
- Proprietary 200 Mbps Marvell MII (MMII) interface
- Dedicated DMA for data movement between memory and port
- Priority queuing on receive based on DA, VLAN Tag, and IP TOS
- Layer 2/3/4 frame encapsulation detection
- TCP/IP checksum on receive and transmit
- DA address filtering

- **USB 2.0 ports (2 ports)**
  - Each port can serve as a peripheral or host
  - USB 2.0 compliant
  - Integrated USB 2.0 PHY
  - EHCI compatible as a host
  - As a host, supports direct connection to all peripheral types (LS, FS, HS)
  - As a peripheral, connects to all host types (HS, FS) and hubs
  - Up to four independent endpoints supporting control, interrupt, bulk, and isochronous data transfers
  - Dedicated DMA for data movement between memory and port
- **Two-Wire Serial Interface (TWSI)**
  - Master/slave operation
  - Serial ROM initialization
- **Two UART interfaces**
  - 16550 UART compatible
  - Two pins for transmit and receive operations
  - Two pins for modem control functions
- **Device bus controller**
  - 8-/16-bit width
  - 166 MHz clock frequency
  - 3.3V I/Os
  - Supports many types of standard memory devices such as FLASH and ROM
  - Four chip selects with programmable timing
  - Optional external wait-state support
  - Boot ROM support
- **NAND Flash support**
  - Glueless interface to CE don't care NAND Flash through the device bus interface
  - Glueless interface to CE care NAND Flash through the device bus and MPP interfaces
  - Boot from NAND Flash when the 1st block, placed on 00h block address, is guaranteed to be a valid block with no errors
  - Support read bursts of up to 128 bytes
- **Four channel Independent DMA controller**
  - Chaining via linked-lists of descriptors
  - Moves data from any to any interface
  - Supports increment or hold on both source and destination address
- **Two XOR DMAs**
  - Useful for RAID application
  - Supports XOR operation on up to eight source blocks
  - Supports CRC-32 calculation
- **Cryptographic engine**
  - Hardware implementation on encryption and authentication engines to boost packet processing speed
  - Dedicated DMA to feed the hardware engines with data from internal SRAM memory
  - Implements AES, DES and 3DES encryption algorithms
  - Implements SHA1 and MD5 authentication algorithms
- **26 multi-purpose pins dedicated for peripheral functions and general purpose I/O**
  - Each pin can be configured independently
  - GPIO inputs can be used to register interrupts from external devices and to generate maskable interrupts
- **Interrupt controller**
  - Maskable interrupts to Feroceon CPU core
  - In endpoint mode, maskable interrupts to the PCI/PCI Express interfaces
- **Timers**
  - Two general purpose 32-bit timer/counters
  - One 32-bit Watchdog timer
- **Internal Architecture**
  - AHB bus for high-performance, low latency Feroceon CPU core to DDR SDRAM connectivity
  - Advanced Mbus architecture with any to any concurrent I/O connectivity
  - Dual port DDR SDRAM controller connectivity to both AHB and Mbus
- **Bootable from**
  - Device interface
  - PCI interface
  - DDR interface
- **HSBGA, 23x23 mm, 388L package, 1 mm ball pitch**

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Preface

About This Document

This datasheet provides the hardware specifications for the Marvell® 88F5182 Feroceon® Storage Networking SoC. The hardware specifications include detailed pin information, configuration settings, electrical characteristics, and physical specifications.

This document is intended to be the basic source of information for designers of new systems.

Related Documentation

The following documents contain additional information related to the 88F5182:

- *88F5182 User Manual,* Doc. No. MV-S103345-01
- *Orion SoC Hardware Design Guide*, Doc. No. MV-S103315-00[1]
- *88F5182 Feroceon Storage Networking SoC Functional Errata, Guidelines, and Restrictions*, Doc. No. MV-S500802-00
- *ARM Architect Reference Manual*, Second Edition
- *AMBA™ Specification*, Rev 2.0
- *PCI Local Bus Specification*, Revision 2.2
- *PCI Express Base Specification*, Revision 1.0a
- Serial-ATA II Phase 1.0 Specification (Extension to SATA I Specification)
- *Universal Serial Bus Specification, Revision 2.0*, April 2000, Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, Philips http://www.usb.org
- *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 0.95, November 2000, Intel Corporation http://www.intel.com
- *USB-HS High-Speed Controller Core* reference[1]
- *RFC 1321* (The MD5 Message-Digest Algorithm)
- *FIPS 180-1* (Secure Hash Standard)
- *FIPS 46-2* (Data Encryption Standard)
- *FIPS 81* (DES Modes of Operation)
- *RFC 2104* (HMAC: Keyed-Hashing for Message Authentication).
- *RFC 2405* – The ESP DES-CBC Cipher Algorithm With Explicit IV
- *RFC 1851* – The ESP Triple DES Transform
- *FIPS draft* - Advanced Encryption Standard (Rijndeal)
- AN-123 Power Sequencing for Marvell Devices, Rev. A (Doc. No. MV-S300427-00)[1]

See the Marvell Extranet website for the latest product documentation.

1. This document is a Marvell proprietary confidential document requiring an NDA and can be downloaded from the Marvell Extranet.

Document Conventions

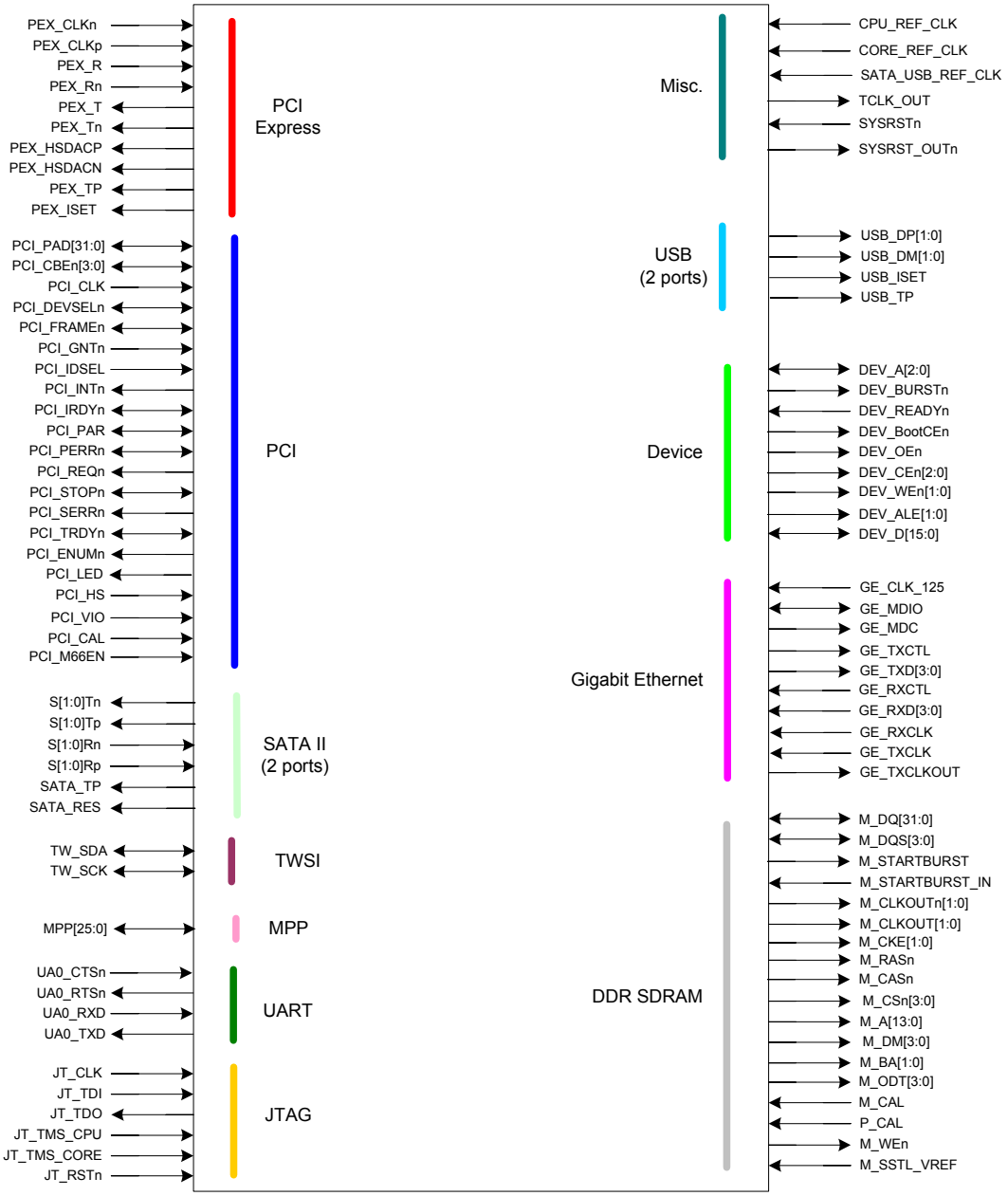
The following conventions are used in this document:

Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Gb: gigabit GB: gigabyte Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Pin Information

1.1 Pin Logic

Figure 1: 88F5182 Interface Pin Logic Diagram



1.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 1 defines the abbreviations and acronyms used in the pin description tables..

Table 1: Pin Functions and Assignments Table Key

Abbreviation	Description
I	Input
O	Output
I/O	Input/Output
t/s	Tri-State pin
s/t/s	Sustained Tri-State pin. The pin is driven to its inactive value for one cycle before float. A pull-up is required to sustain the inactive value.
o/d	Open Drain pin. The pin allows multiple drivers simultaneously (wire-OR connection). A pull-up is required to sustain the inactive value.
CML	Current Mode Logic
HCSL	High-speed Current Steering Logic
LVTTL	Low-voltage TTL 3.3V Driver/Receiver
LVCMOS	Low-voltage CMOS 2.5V Driver/Receiver
SSTL	Stub Series Terminated Logic for 1.8/2.5V pad
PCI	PCI pad 3.3V according to the PCI standard
Calib	Calibration pad type
Power	VDD Power Supply
GND	Ground Supply
Analog	Analog Supply
Vref	Reference Voltage

Table 2: Functional Pin List Summary

Interface	Prefix
DDR SDRAM	M_
PCI Express	PEX_
PCI	PCI_
SATA II Port 0/1	S
Gigabit Ethernet	GE_
USB 2.0 Port 0/1	USB_
TWSI	TW_
UART 0/1	UA0_ UA1_
Device Bus	DEV_
MPP	N/A
JTAG	JT_
Misc	N/A

1.2.1 DDR SDRAM Interface Pin Assignments

Table 3: DDR SDRAM Interface Pin Assignments

Pin Name	I/O / Pin Type /Power Rail		Description
M_SSTL_VREF	I	VREF VDD_M	SSTL Reference Voltage Reference voltage for SSTL interface (1.25V for DDR1, 0.9V for DDR2)
M_CLKOUT[1:0] M_CLKOUTn[1:0]	O	SSTL VDD_M	SDRAM Clock Differential SDRAM clock pairs
M_CKE[1:0]	O	SSTL VDD_M	SDRAM Clock Enable Driven high to enable SDRAM clock. Driven low when putting the SDRAM in self refresh mode.
M_RASn	O	SSTL VDD_M	SDRAM Row Address Select Asserted to indicate an active ROW address driven on the SDRAM address lines.
M_CASn	O	SSTL VDD_M	SDRAM Column Address Select Asserted to indicate an active column address driven on the SDRAM address lines.
M_WEn	O	SSTL VDD_M	SDRAM Write Enable Asserted to indicate a write command to the SDRAM.
M_A[13:0]	O	SSTL VDD_M	SDRAM Address Driven during RASn and CASn cycles to generate, together with the bank address bits, the SDRAM address.
M_BA[1:0]	O	SSTL VDD_M	SDRAM Bank Address Driven during RASn and CASn cycles to select one of the four SDRAM virtual banks.
M_CSn[3:0]	O	SSTL VDD_M	SDRAM Chip Selects Asserted to select a specific SDRAM bank.
M_DQ[31:0]	t/s I/O	SSTL VDD_M	SDRAM Data Bus Driven during write to SDRAM. Driven by SDRAM during reads.
M_DQS[3:0]	t/s I/O	SSTL VDD_M	SDRAM Data Strobe • DQS[0] is the strobe for DQ[7:0]. • DQS[1] is the strobe for DQ[15:8]. • DQS[2] is the strobe for DQ[23:16]. • DQS[3] is the strobe for DQ[31:24]. Driven during write to SDRAM. Driven by SDRAM during reads.
M_DM[3:0]	O	SSTL VDD_M	SDRAM Data Mask • DM[0] is the mask for DQ[7:0]. • DM[1] is the mask for DQ[15:8]. • DM[2] is the mask for DQ[23:16]. • DM[3] is the mask for DQ[31:24].

Table 3: DDR SDRAM Interface Pin Assignments (Continued)

Pin Name	I/O / Pin Type /Power Rail		Description
M_STARTBURST	O	SSTL VDD_M	Start Burst Indication of burst start Indicates the entire window of the read transaction. It is a Marvell® proprietary signal. Routes M_STARTBURST signal to the 88F5182 as M_STARTBURST_IN. Refer to the *Orion SoC Hardware Design Guide* for layout considerations.
M_STARTBURST_IN	I	SSTL VDD_M	Start Burst Input
M_ODT[3:0]	O	SSTL VDD_M	SDRAM On Die Termination control Turns on/off SDRAM on die termination resistor. Pin per each SDRAM chip select
M_CAL	I	Calib	SDRAM Auto Calibration input Allows control of the DDR SDRAM interface output buffers' strength. Connect this pin to VDD_M through a resistor. The resistor value determines the drive strength of the output buffer. Refer to the *Hardware Design Guidelines* for this product and also refer to the product's development board schematics.
P_CAL	I	Calib	SDRAM Auto Calibration input for the P-channel transistor only Allows control of the DDR SDRAM interface output buffers' strength. Connect this pin to VSS through a resistor. The resistor value determines the drive strength of the output buffer. Refer to the *Hardware Design Guidelines* for this product and also refer to the product's development board schematics.
VDD_M	I	Power	DDR1/DDR2 SDRAM Interface I/O Supply Voltage

1.2.2 PCI Express Interface Pin Assignments

Table 4: PCI Express Interface Pin Assignments

Pin Name	I/O / Pin Type		Description
PEX_CLKp, PEX_CLKn	I	HCSL	PCI Express Reference Clock Input 100 MHz, differential
PEX_T, PEX_Tn	O	CML	Transmit Lane Differential pair of PCI Express transmit data
PEX_R, PEX_Rn	I	CML	Receive Lane Differential pair of PCI Express receive data
PEX_HSDACP PEX_HSDACN	O	CML	High Speed DAC
PEX_ISET	O	Analog	Current Reference Terminate this pin with a 6.04 kilohm resistor, pulled down.
PEX_TP	O	Analog	Analog Test Point
PEX_AVDD	I	Power	PCI Express PHY quiet power supply 2.5V
PEX_AVDDL	I	Power	PCI Express PHY quiet power supply 1.5V
PEX_AVDDH	I	Power	PCI Express PHY quiet power supply 3.3V

1.2.3 PCI Bus Interface Pin Assignments

NOTE: All PCI pads are 5V tolerant when PCI_VIO is connected to 5V.

Table 5: PCI Bus Interface Pin Assignments

Pin Name	I/O / Pin Type / Power Rail		Description
PCI_CLK	I	PCI VDDO	PCI Clock PCI interface clock up to 66 MHz.
PCI_VIO	I	PCI VDDO	PCI VIO Clamping reference voltage for PCI (3.3V or 5V)
PCI_M66EN	I	PCI VDDO	PCI 66 MHz Enable PCI_M66EN is sampled on reset de-assertion, to determine if it is connected to a 66 MHz bus. If PCI_M66EN is sampled HIGH, the internal PCI interface DLL is enabled.
PCI_PAD[31:0]	t/s I/O	PCI VDDO	PCI Address/Data 32-bit PCI multiplexed address/data bus. Driven by the transaction master during address phase and write data phase. Driven by the target device during read data phase.
PCI_CBEn[3:0]	t/s I/O	PCI VDDO	PCI Command/Byte Enable 4-bit multiplexed command/byte-enable bus, driven by transaction master. Contains the command during the address phase and byte-enable during data phase.
PCI_PAR	t/s I/O	PCI VDDO	PCI Parity (low) Even parity is calculated for PCI_PAD[31:0] and PCI_CBEn[3:0]. Driven by the transaction master for the address phase and the write data phase. This pin is driven by the target for the read data phase.
PCI_FRAMEn	s/t/s I/O	PCI VDDO	PCI Frame Asserted by the transaction master to indicate the beginning of a transaction. The master de-asserts PCI_FRAMEn to indicate that the next data phase is the final data phase transaction.
PCI_IRDYn	s/t/s I/O	PCI VDDO	PCI Initiator Ready Asserted by the transaction master to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_DEVSELn	s/t/s I/O	PCI VDDO	PCI Device Select Asserted by the target of the current access. As a master, the target device is expected to assert PCI_DEVSELn within five bus cycles. Otherwise, it aborts the cycle. As a target, PCI_DEVSELn is asserted at a medium speed; two cycles after the assertion of PCI_FRAMEn.
PCI_STOPn	s/t/s I/O	PCI VDDO	PCI Stop Asserted by target to indicate transaction termination. Used by a target device to generate a Retry, Disconnect, or Target Abort termination signal.

Table 5: PCI Bus Interface Pin Assignments (Continued)

Pin Name	I/O / Pin Type / Power Rail		Description
PCI_TRDYn	s/t/s I/O	PCI VDDO	PCI Target Ready Asserted by the target to indicate it is ready to complete the current data phase of the transaction. A data phase is completed when both PCI_TRDYn and PCI_IRDYn are asserted.
PCI_IDSEL	I	PCI VDDO	PCI Initialization Device Select Asserted to act as a target device chip select during PCI configuration transactions.
PCI_REQn/PCI_GNTn[1]	t/s O	PCI VDDO	PCI Bus Request When using an external PCI arbiter, this pin is asserted to request PCI bus mastership to initiate a new transaction.
			PCI Device1 Grant When using the internal PCI Arbiter, the internal PCI controller is connected as agent0, and this pin functions as PCI Arbiter Grant for Agent1.
PCI_GNTn/PCI_REQn[1]	I	PCI VDDO	PCI Bus Grant When using an external PCI arbiter, this pin is asserted to indicate that bus mastership is granted.
			When using the internal PCI Arbiter, the internal PCI port is connected as agent0, and this pin functions as PCI Arbiter Request of Agent1.
PCI_PERRn	s/t/s I/O	PCI VDDO	PCI Parity Error Asserted when a data parity error is detected. Asserted by a target device in response to bad address or write data parity, or by master device in response to bad read data parity.
PCI_SERRn	o/d O	PCI VDDO	PCI System Error Asserted when a serious system error (not necessarily a PCI error) is detected.
PCI_INTn	o/d O	PCI VDDO	PCI Interrupt Request Asserted when one of the unmasked internal interrupt sources is asserted. If MSI is enabled, PCI_INTn is not asserted.
PCI_CAL	I	PCI VDDO	PCI Auto Calibration input. Tie to VDDO through a reference resistor externally.
PCI_HS	I	PCI VDDO	CompactPCI Handle Switch Compact PCI Hot Swap Handle Switch Sampled handle switch status to identify board insertion or removal.
PCI_ENUMn	o/d O	PCI VDDO	CompactPCI ENUM interrupt Compact PCI Hot Swap ENUMn interrupt. If ENUM is enabled, this pin is asserted during hot swap insertion or removal.
PCI_LED	t/s O	PCI VDDO	CompactPCI LED On/Off Compact PCI Hot Swap LED turn on/off.

1.2.4 SATA II Interface

Table 6: SATA II Interface Pin Assignment

Pin Name	I/O / Pin Type / Power Rail		Full Name	Description
S[1:0]Tp	O	CML	SATA II of Port x Transmit (+)	Transmit data: Differential analog output of SATA II ports [1:0].
S[1:0]Tn	O	CML	SATA II of Port x Transmit (-)	
S[1:0]Rp	I	CML	SATA II of Port x Receive (+)	Receive data: Differential analog input of SATA II ports [1:0] (Type I).
S[1:0]Rn	I	CML	SATA II of Port x Receive (-)	
SATA_TP	O	Analog	SATA II Test Point	For internal use. Leave this pin unconnected.
SATA_RES	O	Analog	SATA II Resistor	Resistor for the SATA II supply reference. Terminate this pin with a 6.04 kΩ resistor, pulled down.

1.2.5 Gigabit Ethernet Port Interface Pin Assignments

Table 7: Gigabit Ethernet Port Interface Pin Assignment

Pin Name	I/O / Pin Type / Power Rail		Full Name	Description
GE_TXCLKOUT	t/s O	CMOS VDD_GE	RGMII Transmit Clock	RGMII transmit reference output clock for GE_TXD[3:0] and GE_TXCTL Provides 125 MHz, 25 MHz or 2.5 MHz clock. Not used in MII mode.
			GMII Transmit Clock	Provides the timing reference for the transfer of the GE_TXEN, GE_TXERR, and GE_TXD[7:0] signals. This clock operates at 125 MHz.
GE_TXCLK	I	CMOS VDD_GE	MII Transmit Clock	MII transmit reference clock from PHY. Provides the timing reference for the transmission of the GE_TXEN and GE_TXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz.
GE_TXD[3:0]	t/s O	CMOS VDD_GE	RGMII Transmit Data	Contains the transmit data nibble outputs that run at double data rate with bits [3:0] presented on the rising edge of GE_TXCLKOUT and bits [7:4] presented on the falling edge.
			GMII Transmit Data	Contains the transmit data nibble outputs
			MII Transmit Data	MII Transmit Data Contains the transmit data nibble outputs that are synchronous to the GE_TXCLK input.
GE_TXD[7:4]	t/s O	CMOS VDDO	GMII Transmit Data	Contains the transmit data nibble outputs. **NOTE:** Multiplexed on MPP.
GE_TXCTL/ GE_TXEN	t/s O	CMOS VDD_GE	RGMII Transmit Control	Transmit control synchronous to the GE_TXCLKOUT output rising/falling edge. GE_TXEN is presented on the rising edge of GE_TXCLKOUT. A logical derivative of GE_TXEN and GE_TxER is presented on the falling edge of GE_TXCLKOUT.
			GMII Transmit Enable	Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE_TXCLKOUT.
			MII Transmit Enable	Indicates that the packet is being transmitted to the PHY. It Is synchronous to GE_TXCLKOUT.
GE_TXERR	t/s O	CMOS VDDO	MII Transmit Error	It is synchronous to GE_TXCLK. **NOTE:** Multiplexed on MPP.
			GMII Transmit Error	It Is synchronous to GE_TXCLKOUT. **NOTE:** Multiplexed on MPP.

Table 7: Gigabit Ethernet Port Interface Pin Assignment (Continued)

Pin Name	I/O / Pin Type / Power Rail		Full Name	Description
GE_CRS	I	CMOS VDDO	MII Carrier Sense	Indicates that the receive medium is non-idle. In half-duplex mode, GE_CRS is also asserted during transmission. GE_CRS is not synchronous to any clock. **NOTE:** Multiplexed on MPP.
			GMII Carrier Sense	**NOTE:** Multiplexed on MPP.
GE_RXD[3:0]	I	CMOS VDD_GE	RGMII Receive Data	Contains the receive data nibble inputs that are synchronous to GE_RXCLK input rising/falling edge.
			MII Receive Data	Contains the receive data nibble inputs that are synchronous to GE_RXCLK input.
			GMII Receive Data	Contains the receive data nibble inputs.
GE_RXD[7:4]	I	CMOS VDDO	GMII Transmit Data	Contains the receive data nibble outputs. **NOTE:** Multiplexed on MPP.
GE_RXERR	I	CMOS VDDO	MII Receive Error	Indicates that an error symbol, a false carrier, or a carrier extension symbol is detected on the cable. It is synchronous to GE_RXCLK input. **NOTE:** Multiplexed on MPP.
			GMII Receive Error	**NOTE:** Multiplexed on MPP.
GE_RXCTL/ GE_RXDV	I	CMOS VDD_GE	RGMII Receive Control	GE_RXCTL is presented on the rising edge of GE_RXCLK. A logical derivative of GE_RXDV and GE_RXERR is presented on the falling edge of RXCLK.
			MII Receive Data Valid	Indicates that valid data is present on the GE_RXD lines. It is synchronous to GE_RXCLK.
			GMII Receive Data Valid	GMII Receive Data Valid.
GE_RXCLK	I	CMOS VDD_GE	RGMII Receive Clock	The receive clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock derived from the received data stream.
			MII Receive Clock	Provides the timing reference for the reception of the GE_RXDV, GE_RXERR, and GE_RXD[3:0] signals. This clock operates at 2.5 MHz or 25 MHz
			GMII Receive Clock	Provides the timing reference for the reception of the GE_RXDV, GE_RXERR, and GE_RXD[7:0] signals. This clock operates at 125 MHz

Table 7: Gigabit Ethernet Port Interface Pin Assignment (Continued)

Pin Name	I/O / Pin Type / Power Rail		Full Name	Description
GE_COL	I	CMOS VDDO	MII Collision Detect	Indicates a collision has been detected on the wire. This input is ignored in full-duplex mode. GE_COL is not synchronous to any clock. **NOTE:** If not using the MII interface, this pin must be left unconnected. Multiplexed on MPP.
			GMII Collision Detect	**NOTE:** Multiplexed on MPP.
GE_CLK_125	I	CMOS VDD_GE	RGMII Clock	Transmit Reference clock of 125 MHz that is used to generate GE_TXCLKOUT of 125 MHz, 25 MHz or 2.5 MHz.
			GMII Clock.	GMII Clock.
GE_MDC	t/s O	CMOS VDD_GE	Management Data Clock	MDC is the CLK input divided by 64. Provides the timing reference for the transfer of the MDIO signal.
GE_MDIO	t/s I/O	CMOS VDD_GE	Management Data In/Out	Used to transfer control information and status between PHY devices and the GbE controller. **NOTE:** When working with the SMI interface, connect the MDIO signal to a pull up resistor.

Note

The following pins are multiplexed on MPP pins: GE_TXD[7:4], GE_RXD[7:4], GE_TXERR, GE_RXERR, GE_CRS, GE_COL.

1.2.6 USB 2.0 Interface Pin Assignments

Table 8: USB 2.0 Interface Pin Assignments—Two Ports

Pin Name	I/O / Pin Type		Description
USB_DP[1:0], USB_DM[1:0]	I/O	CML	USB 2.0 port data+ and data- pair for ports 0 and 1
USB_TP	O	Analog	Analog Test Point
USB_ISET	O	Analog	Current Reference Terminate this pin with a 6.04 kilohm resistor, pulled down.
USB_AVDD	I	Power	USB 2.0 PHY quiet power supply

1.2.7 TWSI Interface Pin Assignment

Table 9: TWSI Interface Pin Assignment

Pin Name	I/O / Pin Type / Power Rails		Description
TW_SDA	o/d I/O	LVTTL VDDO	TWSI port SDA Address or write data driven by the TWSI master or read response data driven by the TWSI slave.
TW_SCK	o/d I/O	LVTTL VDDO	TWSI port Serial Clock Serves as output when acting as an TWSI master. Serves as input when acting as an TWSI slave.

1.2.8 UART Interface Pin Assignment

Table 10: UART0/1 Interface

Pin Name	I/O / Pin Type / Power Rails		Description
UA0_RXD	I	LVTTL VDDO	RX Data port 0
UA0_TXD	O	LVTTL VDDO	TX Data port 0
UA0_CTSn	I	LVTTL VDDO	Clear To Send port 0
UA0_RTSn	O	LVTTL VDDO	Ready To Send port 0
UA1_RXD	I	LVTTL VDDO	RX Data port 1 **NOTE:** Multiplexed on MPP (see Section 3.1, MPP Multiplexing, on page 33).
UA1_TXD	O	LVTTL VDDO	TX Data port 1 **NOTE:** Multiplexed on MPP (see Section 3.1, MPP Multiplexing, on page 33).
UA1_CTSn	I	LVTTL VDDO	Clear To Send port 1 **NOTE:** Multiplexed on MPP (see Section 3.1, MPP Multiplexing, on page 33).
UA1_RTSn	O	LVTTL VDDO	Ready To Send port 1 **NOTE:** Multiplexed on MPP (see Section 3.1, MPP Multiplexing, on page 33).

1.2.9 MPP Interface Pin Assignment

Table 11: MPP Interface Pin Assignment

Pin Name	I/O / Pin Type / Power Rail		Description
MPP[25:0]	t/s I/O	LVTTL VDDO	Multi Purpose Pin Various functionalities

NOTE: The UART1 port pins are multiplexed on MPP[19:16].

1.2.10 Device Bus Interface Pin Assignments

Table 12: Device Bus Interface Pin Assignments

Pin Name	I/O / Pin Type / Power Rail		Description
DEV_CEn[2:0]	O	LVTTL VDDO	Device Bus Chip Enable corresponds to Bank [2:0]
DEV_BootCEn	O	LVTTL VDDO	Device Bus Boot Chip Enable corresponds to Boot Bank
DEV_OEn	O	LVTTL VDDO	Device Bus Output Enable **NOTE:** DEV_A[15] is multiplexed on DEV_OEn. For additional information, refer to the User Manual.
DEV_WEn[1:0]	O	LVTTL VDDO	Device Bus Byte Write Enable **NOTE:** DEV_A[16] is multiplexed on DEV_WEn[0]. For additional information, refer to the User Manual.
DEV_ALE[1:0]	O	LVTTL VDDO	Device Bus Address Latch Enable
DEV_D[7:0]	t/s I/O	LVTTL VDDO	Device Bus Multiplexed Address/Data bus **NOTE:** DEV_A[13:6] and DEV_A[26:19] are multiplexed on DEV_D[7:0]. For additional information, refer to the User Manual.
DEV_D[15:8]	t/s I/O	LVTTL VDDO	Device Bus Data bus **NOTE:** Pins DEV_A[14] and DEV_A[15] are multiplexed on DEV_D[8]. For additional information, refer to the User Manual.
DEV_A[2:0]	t/s I/O	LVTTL VDDO	Device Bus Address bus **NOTE:** DEV_A[5:3] and DEV_A[18:16] are multiplexed on DEV_A[2:0]. For additional information, refer to the User Manual.
DEV_READYn	I	LVTTL VDDO	Device READY **NOTE:** When not in use, must be pulled down to GND.
DEV_BURSTn/ DEV_LASTn	O	LVTTL VDDO	Device Burst/Device Last
TCLK_OUT	O	LVTTL VDDO	Core Clock Output 166 MHz Device bus clock.

1.2.11 JTAG Interface Pin Assignment

Table 13: JTAG Pin Assignment

Pin Name	I/O / Pin Type / Power Rail		Description
JT_CLK	I	PCI VDDO	JTAG Clock Clock input for the JTAG controller. **NOTE:** This pin is internally pulled down to 0.
JT_RSTn	I	PCI VDDO	JTAG Reset When asserted, resets the JTAG controller. **NOTE:** This pin is internally pulled down to VSS.[1]
JT_TMS_CPU	I	PCI VDDO	CPU JTAG Mode Select Controls the CPU JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TMS_CORE	I	PCI VDDO	Core JTAG Mode Select Controls the Core JTAG controller state. Sampled with the rising edge of JT_CLK. **NOTE:** This pin is internally pulled up to 1.
JT_TDO	O	PCI VDDO	JTAG Data Out Driven on the falling edge of JT_CLK.
JT_TDI	I	PCI VDDO	JTAG Data In JTAG serial data input. Sampled with the JT_CLK rising edge. **NOTE:** This pin is internally pulled up to 1.

1. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles.

Note

All JTAG pads are 5V tolerant when PCI_VIO is connected to 5V.

1.2.12 Miscellaneous Pin Assignment

The Miscellaneous signal list contains clock and reset and related signals.

Table 14: Miscellaneous Pin Assignments

Pin Name	I/O / Pin Type / Power Rail		Description
CORE_REF_CLK	I	LVTTL T_AVDD	Core Clock (TCLK) Reference Clock 25 MHz Reference clock for TCLK PLL. **NOTE:** Core Clock (TCLK) provides the clock to the internal Mbus interface, to the Device bus interface and to the MPP interface. This pin is configurable at reset, see PLL clock reference pins in Table 20, Reset Configuration, on page 41.
CPU_REF_CLK	I	LVTTL S_AVDD	CPU Reference Clock 25 MHz Reference clock for CPU PLL. **NOTE:** CPU_REF_CLK provides the clock to the Feroceon™ core, the AHB bus, the AHB2M bridge and the SDRAM controller. This pin is configurable at reset, see PLL clock reference pins in Table 20, Reset Configuration, on page 41.
S_AVDD	I	Power	SysCLK PLL quiet power supply 3.3V
S_AVSS	I	GND	SysCLK PLL quiet VSS
T_AVDD	I	Power	TCLK PLL quiet power supply 3.3V
T_AVSS	I	GND	TCLK PLL quiet VSS
SATA_USB__REF_CLK	I	LVTTL USB_VDD	USB 2.0 port and SATA port reference clock. 25 MHz. **NOTE:** This pin is configurable at reset, see PLL clock reference pins in Table 20, Reset Configuration, on page 41.
SYSRSTn	I	LVTTL VDDO	System Reset Main reset signal of the device. Used to reset all units to their initial state. When in the reset state, all output pins are in tri-state.
SYSRST_OUTn	o/d O	LVTTL VDDO	Reset request indication from the device to external reset hardware. Open drain output, which is pulled-up by the internal pull-up in the 88F5182. This configuration allows connecting the signal without having to add additional logic to the hardware reset module on the board.

1.3 Internal Pull-up and Pull-down Pins List

Some pins of the device package are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 150 kilohms. An external resistor with a lower value can
override this internal resistor.

The internal pull-up or pull-down status for each relevant pin is listed in Table 15.

Table 15: Internal Pull-up and Pull-down Pins List

Pin Name	Pin #	Pull-up/Pull-down
DEV_BURST	D22	Pull-up
DEV_Oen	F19	Pull-down
DEV_Wen[1]	G19	Pull-down
DEV_Wen[0]	G20	Pull-down
DEV_ALE[1]	G21	Pull-down
DEV_ALE[0]	G22	Pull-down
DEV_D[8]	H19	Pull-up
DEV_D[7]	H20	Pull-up
DEV_D[6]	H21	Pull-down
DEV_D[5]	H22	Pull-up
DEV_D[4]	J19	Pull-up
DEV_D[3]	J20	Pull-up
DEV_D[2]	J22	Pull-up
DEV_D[1]	K19	Pull-down
DEV_D[0]	K20	Pull-down
DEV_A[2]	K21	Pull-down
DEV_A[1]	K22	Pull-down
DEV_A[0]	L19	Pull-down
DEV_D[15]	L20	Pull-down
DEV_D[14]	L21	Pull-up
DEV_D[13]	L22	Pull-down
DEV_D[9]	M19	Pull-up
DEV_D[10]	M20	Pull-up
DEV_D[11]	M21	Pull-down
DEV_D[12]	M22	Pull-down
JT_TDI	W5	Pull-up
JT_TMS_CORE	Y4	Pull-up
JT_RSTn	AA1	Pull-down
JT_CLK	AB1	Pull-down
JT_TMS_CPU	AB2	Pull-up
SYSRST_OUTn	AB3	Pull-up

2 88F5182 Pin Map and Pin List

The 88F5182 pin list is provided as an Excel file attachment.

To open the attached Excel pin list file, double-click the pin icon below:

88F5182_Pinout_External.xls

NOTE: The file attachment is only supported by Adobe Reader 6.0 and above.

3 Pin Multiplexing

3.1 MPP Multiplexing

The 88F5182 device contains 26 Multi Purpose Pins (MPP). Each one can be assigned to a different functionality through the MPP Control register.

- GPIO: General Purpose In/Out Port, see the General Purpose I/O Port section in the *88F5182 User Manual.*
- PCI_REQn[5:2]/PCI_GNTn[5:2]: PCI Arbitration Signals, see the PCI Interface section in the *88F5182 User Manual.*
- PCI_PMEn: PCI Power Management Event—see the PCI interface section in the *88F5182 User Manual.*
- GE_TXD[7:4]/GE_RXD[7:4]: GbE port Signals when configured to GMII interface—see the Gigabit Ethernet Controller section in the *88F5182 User Manual*.
- GE_TXER, GE_RXER, GE_CRS, GE_COL: GbE port Signals when configured to GMII or MII interface.
- M_BB: SDRAM battery backup trigger.
- PEX_RST_OUTn: Optional PCI Express boards reset output.
- UA1_RXD, UA1_TXD, UA1_CTSn, UA1_RTSn: UART1 pins.
- PCI output clock
- Standard NAND Flash pins

Table 16 shows MPP[19:0] pins' functionality as determined by the MPP Multiplex register—see the Pins Multiplexing Interface Registers section in the *88F5182 User Manual*.

- MPP[21:20] functionality is determined according to section Section 5.5, Pins Sample Configuration, on page 41 to be either PCI clock out or GPIO[21:20].
- MPP[25:22] always function as GPIO[25:22].

Table 16: MPP Function Summary

MPP Pin[1]	0x0	0x1	0x2	0x3	0x4	0x5
MPP[0]	PEX_RST_OUTn		PCI_REQn[2] (in)	GPIO[0] (in/out)		
MPP[1]	GPIO[1] (in/out)		PCI_GNTn[2] (out)			
MPP[2]	GPIO[2] (in/out)		PCI_REQn[3] (in)	PCI_PMEn (out)		
MPP[3]	GPIO[3] (in/out)		PCI_GNTn[3] (out)			
MPP[4]	GPIO[4] (in/out)		PCI_REQn[4] (in)		BOOT NAND Flash REn	SATA 0 presence indication (Active Low)

Table 16: MPP Function Summary (Continued)

MPP Pin[1]	0x0	0x1	0x2	0x3	0x4	0x5
MPP[5]	GPIO[5] (in/out)		PCI_GNTn[4] (out)		BOOT NAND Flash WEn	SATA 1 presence indication (Active Low)
MPP[6]	GPIO[6] (in/out)		PCI_REQn[5] (in)		NAND Flash REn[0]	SATA 0 active indication (Active Low)
MPP[7]	GPIO[7] (in/out)		PCI_GNTn[5] (out)		NAND Flash WEn[0]	SATA 1 active indication (Active Low)
MPP[8]	GPIO[8] (in/out)	GE_COL (in)				
MPP[9]	GPIO[9] (in/out)	GE_RXERR (in)				
MPP[10]	GPIO[10] (in/out)	GE_CRS (in)				
MPP[11]	GPIO[11] (in/out)	GE_TXERR (out)				
MPP[12]	GPIO[12] (in/out)	GE_TXD[4] (out)			NAND Flash REn[1]	SATA 0 presence LED indication (Active Low))
MPP[13]	GPIO[13] (in/out)	GE_TXD[5] (out)			NAND Flash WEn[1]	SATA 1 presence LED indication (Active Low)
MPP[14]	GPIO[14] (in/out)	GE_TXD[6] (out)			NAND Flash REn[2]	SATA 0 active LED indication (Active Low)
MPP[15]	GPIO[15] (in/out)	GE_TXD[7] (out)			NAND Flash WEn[2]	SATA 1 active LED indication (Active Low)
MPP[16]	UA1_RXD (in)	GE_RXD[4] (in)				GPIO[16] (in/out)
MPP[17]	UA1_TXD (out)	GE_RXD[5] (in)				GPIO[17] (in/out)
MPP[18]	UA1_CTSn (in)	GE_RXD[6] (in)				GPIO[18] (in/out)
MPP[19]	UA1_RTSn (out)	GE_RXD[7] (in)				GPIO[19] (in/out)

1. MPP[7:0] are 5V tolerant when PCI_VIO is connected to 5V.

Note

- Depending on its configured functionality, each pin acts as either an output or input pin. All the MPP pins wake up after reset in 0x0 mode: MPP[0] wakes up as PEX_RST_OUTn after reset, MPP[15:1] pins wake up after reset as GPIO input pins, and MPP[19:16] wake up as UART1 pins after reset.
- Pins that are left as GPIO (for MPP[15:8]) and are not connected should be set to output after SYSRST de-assertion.

3.2 Gigabit Ethernet (GbE) Pins Multiplexing on MPP

The 88F5182 has 16 dedicated pins for its GbE port. The port can be configured to have MII/GMII/RGMII interface to the external PHY or switch device. When configured to GMII, GE_TXD[7:4]/GE_RXD[7:4] pins are multiplexed on the MPP. When configured to GMII or MII, GE_TXER, GE_RXER, GE_CRS, GE_COL pins are multiplexed on the MPP.

Table 17 lists the GbE port pins multiplexing.

Table 17: Ethernet Port Pins Multiplexing

Pin Name	GMII	MII	RGMII
GE_TXCLK		GE_TXCLK (in)	
GE_TXCLKOUT	GE_TXCLKOUT (out)		GE_TXCLKOUT (out)
GE_TXD[3:0]	GE_TXD[3:0] (out)	GE_TXD[3:0] (out)	GE_TXD[3:0] (out)
GE_TXEN	GE_TXEN (out)	GE_TXEN (out)	GE_TXCTL (out)
GE_RXD[3:0]	GE_RXD[3:0] (in)	GE_RXD[3:0] (in)	GE_RXD[3:0] (in)
GE_RXDV	GE_RXDV (in)	GE_RXDV (in)	GE_RXCTL (in)
GE_RXCLK	GE_RXCLK (in)	GE_RXCLK (in)	GE_RXCLK (in)
MPP[15:12]	GE_TXD[7:4] (out)		
MPP[19:16]	GE_RXD[7:4] (in)		
MPP[11]	GE_TXERR (out)	GE_TXERR (out)	
MPP[9]	GE_RXERR (in)	GE_RXERR (in)	
MPP[10]	GE_CRS (out)	GE_CRS (out)	
MPP[8]	GE_COL (in)	GE_COL (in)	
GE_CLK125	GE_CLK125 (in)		GE_CLK125 (in)
GE_MDC (out)	GE_MDC (out)	GE_MDC (out)	GE_MDC (out)
GE_MDIO (out)	GE_MDIO (out)	GE_MDIO (out)	GE_MDIO (out)

4 Clocking

4.1 Reference Clocks

The following table lists the clocks.

Table 18: Reference Clocks

PLL/DLL	Description
CPU PLL	■ One of the following pins is determined as the reference clock according to Section 5.5, Pins Sample Configuration, on page 41 • CPU_REF_CLK (25 MHz) or • SATA_USB_REF_CLK(25 MHz) or ■ Derivative clocks • CPU Clock • DDR Clock (The AHB bus uses the DDR clock.)
Core PLL	■ One of the following pins is determined as the reference clock according to Section 5.5, Pins Sample Configuration, on page 41 • CPU_REF_CLK (25 MHz) or • SATA_USB_REF_CLK(25 MHz) or • CORE_REF_CLK (25 MHz) ■ Derivative clocks • TCLK
PEX PLL	■ Reference clock • PEX_CLKp, PEX_CLKn (100 MHz) differential clock ■ Derivative clocks • PEX Clock
SATA PLL/USB PLL	■ Reference clock • SATA_USB_REF_CLK(25 MHz) ■ Derivative clocks • SATACLK • USBCLK
PCI DLL	■ Reference clock • Clock is derived directly from PCI_CLK, running at the PCI interface frequency (66/33 and below MHz) ■ Derivative clocks • None.

The function of each CPU/DDR Clock Frequency Ratio mode is defined in field CPU/DDR Clock Frequency Ratio after reset (see CPU/DDR Clock Frequency Ratio in Table 20, Reset Configuration, on page 41).

4.2 Output Clocks

The 88F5182 has the following output clocks:

- The TCLK_OUT pin outputs TCLK.
- PCI clock is generated from Core PLL and multiplexed on MPP[21:20].

5 Reset Configuration

5.1 Hardware Reset

The 88F5182 has one reset input pin—SYSRSTn. When asserted, the entire chip is placed in its initial state. All outputs except some DRAM interface output pins are placed in high-z.

The following output pins are still active during SYSRSTn assertion:

- GE_TXCLKOUT
- M_CLKOUT[1:0], M_CLKOUTn[1:0]
- M_CKE[1:0]
- M_ODT[3:0]
- M_STARTBURST
- DEV_CEn[2:0]
- DEV_BootCEn
- TCLK_OUT
- MPP[21:20]

Note

Pins MPP[21:20] only remain active during SYSRSTn assertion when DEV_D[14] is pulled up (see Table 20, Reset Configuration, on page 41).

The 88F5182 has an SYSRST_OUTn output signal that is used as a reset request from the 88F5182 to the board reset logic. This signal is set when one of the following maskable events occurs:

- Received hot reset indication from the PCI Express link (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the *88F5182 User Manual*). In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles.
- PCI Express link failure (only relevant when used as a PCI Express endpoint), and bit <PexRstOutEn> is set to 1 in the RSTOUTn Mask Register. In this case, SYSRST_OUTn is asserted for duration of ~300 TCLK cycles.
- Watchdog timer expiration and bit <WDRstOutEn> is set to 1 in the RSTOUTn Mask Register.
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register.

Note

Reset must be active for a minimum length of 100 ms. Core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

5.2 PCI Express Reset

The PCI Express specification defines two ways to reset the PCI Express interface. In addition, a link failure condition has a similar affect to a PCI Express reset.

As a root complex the 88F5182 may generate a reset to the PCI Express port in any of the following ways:

Fundamental reset

The board reset logic generates reset signal to the PERST# pin in the PCI Express connector.

The board reset logic must also generate a reset signal to the SYSRSTn pin of the 88F5182. When the SYSRSTn pin is asserted, the entire chip is reset, including the PCI Express interface logic and registers.

Hot reset

Hot reset is triggered by the CPU core by setting the conf_mstr_hot_reset bit in the PCI Express Control Register (see *888F5182 User Manual*).

When Hot reset is triggered, the PCI Express interface is reset. All PCI Express interface registers, except sticky bits, are reset. A maskable interrupt is asserted.

Link fail reset

Link failure is detected when the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state).

When Link failure is detected, the PCI Express interface is reset. A maskable interrupt is asserted.

5.2.1 PCI Express Reset in Endpoint Mode

When working in Endpoint mode, both link fail and hot reset conditions trigger a chip internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.

As a endpoint the 88F5182 receives a reset from the PCI Express port in any of the following ways:

Fundamental reset

Fundamental reset is indicated by the assertion of PERST# pin in the PCI Express connector. The PERST# pin must be connected via the board reset logic to the SYSRSTn input pin. See “Section 5.1, Hardware Reset, on page 38” for further details.

The board reset logic must also generate a reset signal to the rest or the board logic.

When the SYSRSTn pin is asserted, the entire chip is reset, including the PCI Express interface logic and registers.

Hot reset

Hot reset is triggered by the reception of a Hot reset packet from the PCI Express port.

When a Hot reset packet is received, the 88F5182 triggers an internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.

Link fail reset

Link failure is detected when the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state).

When Link failure is detected, the 88F5182 triggers an internal reset. All the chip logic is set back to default values except for sticky registers and the sample on reset logic. In addition MPP[0] is asserted to reset the entire board.

Note

When working in Endpoint mode, clear the following register fields in the PCI Express Debug Control register of the PCI Express interface (see the 88F5182 User Manual):

- <conf_msk_link_fail>
- <conf_msk_hot_reset>
- <conf_dis_link_fail_reg_rst>

The endpoint reset scheme flow appears in Figure 2. Table 19 describes each of the pins mentioned in the figure.

Figure 2: Endpoint Reset Scheme

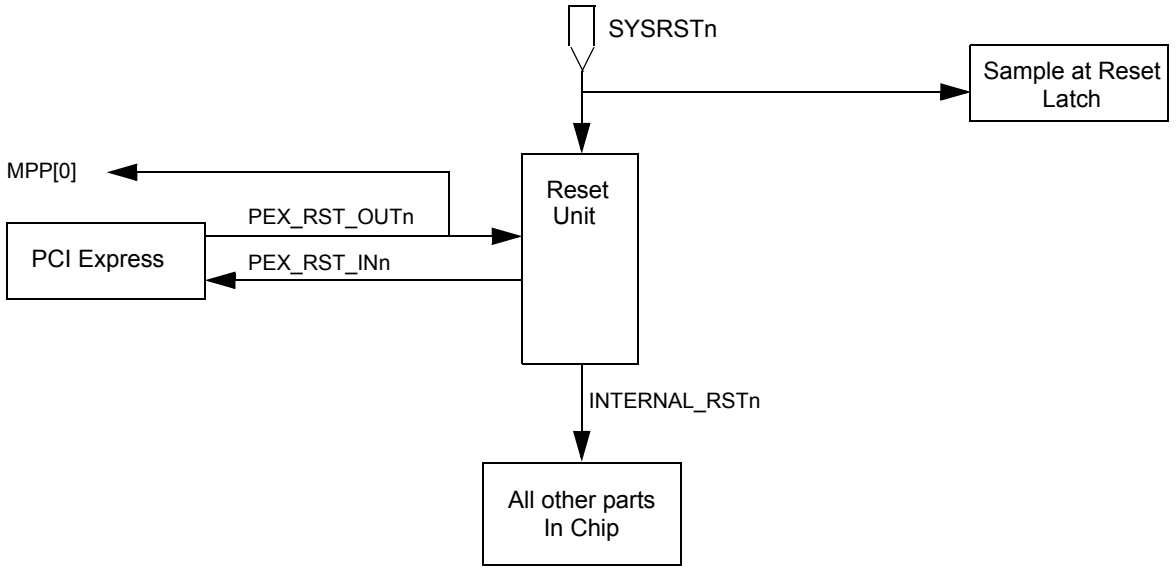


Table 19: Endpoint Reset Scheme

Signal Name	Active
MPP[0]	Active when one of the following occurs: • PEX_RST_OUTn is active.
PEX_RST_OUTn	Active when one of the following occurs: • PEX Link failure occurs and is not masked. • PEX Hot reset occurs and is not masked. **NOTE:** The mask bits are sticky and reset by SYSRSTn only.
PEX_RST_INn	Active when one of the following occurs: • SYSRSTn is asserted (synchronized to TCLK).
INTERNAL_RESET	Active when one of the following occurs: • SYSRSTn is asserted (synchronized to TCLK). • PEX_RST_OUTn is asserted.

5.3 PCI Reset

When working as a PCI add-in card, the PRST# pin in the PCI connector should be connected to the SYSRSTn input pin. See Section 5.1, Hardware Reset, on page 38 for further details.

5.4 Feroceon® CPU Tap Controller Reset

Reset when JT_RSTn is set and JT_TMS_CPU is active.

5.5 Pins Sample Configuration

The following pins are sampled during SYSRSTn de-assertion. Internal pull up/down resisters set the default mode. External pull up/down resisters are required to change the default mode of operation. These signals must remain pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).

Note

- All internal pull up/down resistors are 150 kilohms.
- Most of the reset strapping pins integrate a weak pull-up or pull-down resistor (indicated in Table 20 as pulled up to 1 or pulled down to 0, respectively). When using latches, buffers, or other logic that can change the signal logic level (i.e., bus holders), it is highly recommended to use external resistors (for additional information, refer to the *Orion SoC Hardware Design Guide*).

Table 20: Reset Configuration

Pin	Configuration Function
DEV_D[0]	Serial ROM initialization
	0 = Disabled 1 = Enabled **NOTE:** Internally pulled down to 0.
DEV_D[1]	Watchdog Enable
	0 = Watchdog Disable 1 = Watchdog Enable **NOTE:** Internally pulled down to 0.
DEV_D[3]	PCI Express mode select
	0 = Endpoint 1 = Root Complex **NOTE:** Internally pulled up to 1. When working in Endpoint mode, and expansion ROM is used; expansion ROM parameters need to be configured during the serial initialization phase.
DEV_D[5]	DRAM Type
	0 = DDR1 SDRAM 1 = DDR2 SDRAM **NOTE:** Internally pulled up to 1.
DEV_D[12], DEV_D[15], DEV_D[4], DEV_D[2]	CPU/DDR Clock Frequency Ratio
	0 = 333/167 1 = 400/200 2 = 400/133 3 = 500/167 (Internal default) 4–F = Reserved **NOTE:** Mode[3:0] = DEV_D[12], DEV_D[15], DEV_D[4], DEV_D[2]. The pins are listed in MSB to LSB order.

Table 20: Reset Configuration (Continued)

Pin	Configuration Function
DEV_D[7:6]	TCLK Frequency
	0 = Reserved 1 = 150 MHz 2 = 166 MHz 3 = Reserved **NOTE:** Internally pulled to 0x2.
DEV_D[10:8]	Gigabit Ethernet Port Mode Select
	000 = Unused 001 = Reserved 010 = GMII 011 = MII 100 = Reserved 101 = Reserved 110 = Reserved 111 = RGMII (default) **NOTE:** Internally pulled up to 111.
DEV_D[11]	DEV_BootCEn Device Width
	0 = 8 bits 1 = 16 bits **NOTE:** Internally pulled down to 0.
DEV_D[13]	Big Endian initialization
	0 = Little Endian 1 = Big Endian **NOTE:** Internally pulled down to 0.
DEV_D[14]	PCI clock out enable
	Generate and expose PCI clock out on MPP[20] and MPP[21] 0= GPIO[21:20] are multiplexed on MPP[21:20]. 1= PCI Clock out is driven on MPP[20] and MPP[21]. **NOTE:** Internally pulled down to 0.
DEV_ALE[0]	Reserved
	NOTE: Must be pulled to 1. Internally pulled down to 0.
DEV_ALE[1]	Reserved
	NOTE: Internally pulled down to 0.

Table 20: Reset Configuration (Continued)

Pin	Configuration Function
DEV_A[1:0]	PLL clock reference pins
	Define CPU PLL, Core PLL, USB PLL and SATA PLL clock reference pin(s). 0 = All PLLs use SATA_USB_REF_CLK as reference clock 1 = CPU PLL and Core PLL use CPU_REF_CLK while USB PLL and SATA PLL use SATA_USB_REF_CLK 2 = CPU PLL uses CPU_REF_CLK, core PLL uses CORE_REF_CLOCK, USB PLL and SATA PLL use SATA_USB_REF_CLK 3 = Reserved **NOTE:** Internally pulled down to 0. When the reference clock is not in use, it must be connected to VSS.
DEV_A[2]	Reserved
	Reserved for Marvell usage. Must Sample 0 at reset. **NOTE:** Internally pulled down to 0.
DEV_BURSTn	Reserved
	NOTE: Internally pulled up to 1.
DEV_WEn[0]	Boot from NAND Flash
	Defines the default value of bit <NFBoot> in the NAND Flash Control Register (see the *88F5182 User Manual*) 0 = Boot not from NAND Flash 1 = Boot from NAND Flash **NOTE:** Internally pulled down to 0.
DEV_WEn[1]	Standard NAND Flash (CE care)
	Defines the default value of bit <NFActCEnBoot> in the NAND Flash Control Register (see the *88F5182 User Manual*) 0 = Non-Standard NAND Flash (Boot from CE don't care NAND Flash) 1 = Standard NAND Flash (Boot from CE care NAND Flash) When DEV_WEn[0] and DEV_WEn[1] are both set to 1, fields <MPPSel4> and <MPPSel5> in the MPP Control 0 Register are set to 0x4 (see the *88F5182 User Manual*). These fields are cleared to 0x0 otherwise. **NOTE:** Internally pulled down to 0.
DEV_OEn	Boot NAND Flash Initialize Disabled
	0 = If DEV_WEn[0] is set to 1 and DEV_OEn is clear to 0, the NAND Flash initialization sequence is performed. 1 = The NAND Flash initialization sequence is disabled. **NOTE:** Internally pulled down to 0.

Note

Reset sampled values are registered in the MPP Sample at Reset register.

Part of the PCI interface signals are also sampled on PCI reset de-assertion, as specified in the PCI specification.

Table 21: PCI Reset Configuration

Pin	Configuration Function
PCI_M66EN	PCI 66 MHz Enable
	DLL enable and PCI_Clock out frequency 0 = DLL disable, PCI Clock out = 33 MHz (Core clock/5) 1 = DLL Enable, PCI Clock out = 66 MHz (Core clock/2.5)
PCI_DEVSELn PCI_STOPn PCI_TRDYn	PCI Mode
	111 = Conventional PCI All other values are reserved.

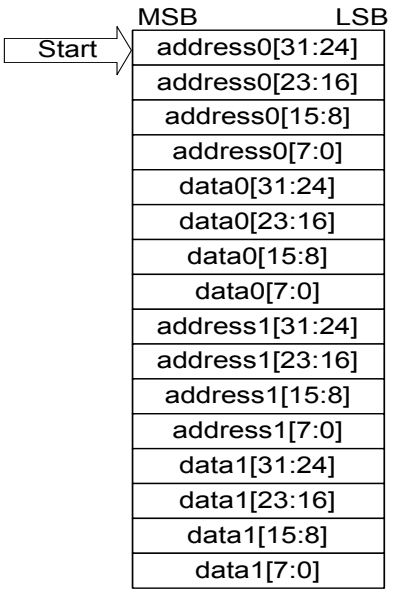
5.6 Serial ROM Initialization

The 88F5182 device supports initialization of ALL of its internal and configuration registers through the TWSI master interface. If serial ROM initialization is enabled, the 88F5182 device TWSI master starts reading initialization data from serial ROM and writes it to the appropriate registers.

5.6.1 Serial ROM Data Structure

Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 3.

Figure 3: Serial ROM Data Structure



The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target. This scheme enables not only programming of the 88F5182 internal registers, but

also initialization of other system components. The only limitation is that it supports only single 32-bit writes (no byte enables nor bursts are supported).

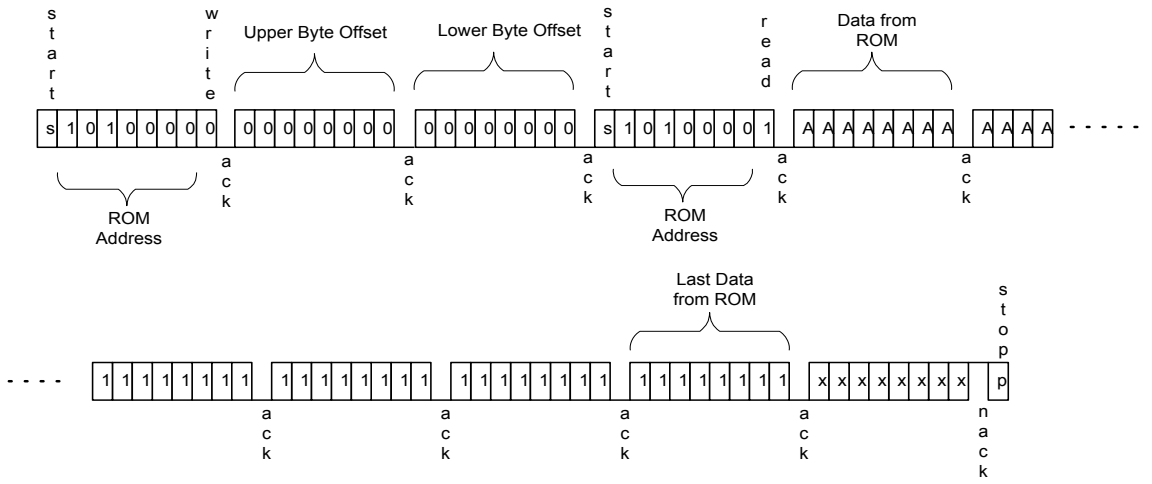
The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the 88F5182 device reaches last data, it stops the initialization sequence.

Note Users must not generate requests through the TWSI auto-loader to addresses that are not 32-bit aligned.

5.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the 88F5182 device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs the sequence of reads, until it reaches last data item, as shown in Figure 4.

Figure 4: Serial ROM Read Example



For a detailed description of TWSI implementation, see the Two-Wire Serial Interface section in the *88F5182 Datasheet Users Manual*.

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The 88F5182 device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the 88F5182 device receives an additional byte of dummy data. It responds with no-ack and then asserts the stop bit.

5.7 Power Sequencing

Refer to *AN-123 Power Sequencing for Marvell Devices* (Doc. No. MV-S300427-00).

6 Electrical Specifications (Preliminary)

Note

The numbers specified in this section are PRELIMINARY and SUBJECT TO CHANGE.

6.1 Absolute Maximum Ratings

Table 22: Absolute Maximum Ratings

Symbol	Min	Max	Units	Parameter
VDD_CORE	-0.5	1.5	V	Core voltage
VDD_CPU	-0.5	1.7	V	CPU core voltage
VDD_M	-0.5	3.0	V	I/O voltage for: DDR1/DDR2 SDRAM interface
M_SSTL_ VREF	-0.5	1.5	V	Reference voltage for: DDR1/DDR2 SDRAM interface
VDDO	-0.5	4.0	V	I/O voltage for: Device, PCI, MPP, JTAG, TWSI, UART, SPI, PCM Interfaces and CORE_REF_CLK, CPU_REF_CLK, and USB_REF_CLK **NOTE:** Input voltage must not exceed the respective interface supply voltage more than 0.7 V.
PEX_AVDDH	-0.5	4.0	V	Analog power supply voltage 1 for: PCI Express PHY
PEX_AVDDL	-0.5	1.8	V	Analog power supply voltage 2 for: PCI Express PHY
PEX_AVDD	-0.5	3.0	V	Analog power supply voltage 3 for: PCI Express PHY
VDD_GE	-0.5	4.0	V	I/O voltage for: RGMII/GMII/MMII/MII/SMI interface
USB_AVDD	-0.5	4.0	V	I/O voltage for: USB interface
SATA_AVDD	-0.5	3.0	V	I/O voltage for: SATA interface
S_AVDD	-0.5	4.0	V	Quiet power supply for: CPU PLL
T_AVDD	-0.5	4.0	V	Quiet power supply for: Core PLL
TC	-40	125	° C	Case temperature
TSTG	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating may damage the device.
- Operation beyond the recommended operating conditions (Table 23) is neither recommended nor guaranteed.

Note Before designing a system, it is recommended that you read application note AN-63: Thermal Management for Marvell Technology Products. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

6.2 Recommended Operating Conditions

Table 23: Recommended Operating Conditions

Symbol	Min	Typ	Max	Units	Parameter
VDD_CORE	1.14	1.2	1.26	V	Core voltage
VDD_CPU	1.34	1.4	1.45	V	CPU core voltage for 500 MHz
	1.14	1.2	1.26	V	CPU core voltage up to 400 MHz
VDD_M	2.3	2.5	2.7	V	I/O voltage for: DDR1 SDRAM interface
	1.7	1.8	1.9	V	I/O voltage for: DDR2 SDRAM interface
M_SSTL_ VREF	0.49* VDD_M	0.5* VDD_M	0.51* VDD_M	V	Reference voltage for: DDR2 SDRAM interface
VDDO	3.15	3.3	3.45	V	I/O voltage for: Device, PCI, MPP, JTAG, TWSI, UART, SPI, PCM interfaces and CORE_REF_CLK, CPU_REF_CLK, and USB_REF_CLK
PEX_AVDDH	3.15	3.3	3.45	V	Analog power supply voltage 1 for: PCI Express PHY
PEX_AVDDL	1.42	1.5	1.575	V	Analog power supply voltage 2 for: PCI Express PHY
PEX_AVDD	2.38	2.5	2.62	V	Analog power supply voltage 3 for: PCI Express PHY
VDD_GE	2.38	2.5	2.62	V	I/O voltage for: RGMII/SMI interface
	3.15	3.3	3.45	V	I/O voltage for: GMII/MMII/MII/SMI interface
USB_AVDD	3.15	3.3	3.45	V	I/O voltage for: USB interface
SATA_AVDD	2.375	2.5	2.625	V	I/O voltage for: SATA interface
S_AVDD	3.15	3.3	3.45	V	Quiet power supply for: CPU PLL

Table 23: Recommended Operating Conditions (Continued)

Symbol	Min	Typ	Max	Units	Parameter
T_AVDD	3.15	3.3	3.45	V	Quiet power supply for: Core PLL
	2.38	2.5	2.62	V	
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

6.3 Thermal Power Dissipation

Table 24: Thermal Power Dissipation

Interface	Symbol	Test Conditions	Typ	Units
Core Digital Power Supply	P_{VDD_CORE}		1000	mW
CPU Digital Power Supply @ 500 MHz	P_{VDD_CPU}	VDD_CPU = 1.4V	1300	mW
CPU Digital Power Supply @ 400 MHz	P_{VDD_CPU}	VDD_CPU = 1.2V	800	mW
RGMII 2.5V interface	P_{VDD_GE}		50	mW
DDR1 DIMM interface parallel termination (32-bit 166 MHz)	P_{VDD_M}	2 single DIMM load	750	mW
DDR2 DIMM interface (32-bit 200 MHz) ODT	P_{VDD_M}	2 single DIMM load, 75 ohm ODT load	750	mW
PCI (66 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	P_{VDDO}	25 pF load	350	mW
PCI (33 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	P_{VDDO}	25 pF load	250	mW
PCI Express interface	P_{PEX}	When the port is not shutdown	120	mW
SATA interface	P_{SATA}	When the port is not shutdown 215 mW per port	430	mW
USB interface	P_{USB}	When the port is not shutdown 120 mW per port	240	mW

Notes:
1. Power in mW is calculated using the typical recommended VDD specification for each power rail.
2. Trace load is 5 pF unless specified otherwise.

6.4 Current Consumption

Table 25: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core Digital Power Supply Current	I_{VDD_CORE}		900	mA
CPU Digital Power Supply Current @ 500 MHz	I_{VDD_CPU}	VDD_CPU = 1.45V	1100	mA
CPU Digital Power Supply Current @ 400 MHz	I_{VDD_CPU}	VDD_CPU = 1.26V	800	mA
RGMII 2.5V interface	I_{VDD_GE}		50	mA
DDR1 DIMM interface parallel termination (32-bit 166 MHz)	I_{VDD_M}	2 single DIMM load	800	mA
DDR2 DIMM interface (32-bit 200 MHz) ODT	I_{VDD_M}	2 single DIMM load, 75 ohm ODT load	650	mA
PCI (66 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	I_{VDDO}	25 pf load	350	mA
PCI (33 MHz 32-bit) interface (including MPP, Device Bus, JTAG, TWSI, and UART)	I_{VDDO}	25 pf load	200	mA
PCI Express interface	I_{PEX_AVDD}	When the port is not shutdown	30	mA
	I_{PEX_AVDDL}		30	mA
	I_{PEX_AVDDH}		10	mA
CPU PLL	I_{S_AVDD}		10	mA
Core PLL	I_{T_AVDD}		10	mA
SATA interface	I_{SATA}	When the port is not shutdown 90 mA per port	180	mA
USB interface	I_{USB}	When the port is not shutdown 40 mA per port	80	mA

Notes:

1. Current in mA is calculated using maximum recommended VDD specification for each power rail.
2. All output clocks toggling at their specified rate.
3. Maximum drawn current from the power supply.
4. Trace load is 5 pF unless specified otherwise.

6.5 DC Electrical Specifications

6.5.1 Reduced Gigabit Media Independent Interface (RGMII) 2.5V DC Electrical Specifications

Table 26: RGMII Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 1 mA	-		0.4	V	-
Output high level	VOH	IOH = -1 mA	2		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.2 Gigabit Media Independent Interface (GMII) 3.3V DC Electrical Specifications

Table 27: GMII Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.3 Media Independent Interface (MII/MMII) 3.3V DC Electrical Specifications

Table 28: MII/MMII Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.4 Serial Management Interface (SMI) 3.3V DC Electrical Specifications

Table 29: SMI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.5 Serial Management Interface (SMI) 2.5V DC Electrical Specifications

Table 30: RGMII Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 1 mA	-		0.4	V	-
Output high level	VOH	IOH = -1 mA	2		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.6 SDRAM DDR1 Interface 2.5V DC Electrical Specifications

Table 31: SDRAM DDR1 Interface 2.5V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		VREF-0.15	V	-
Input high level	VIH		VREF+0.15		VDDIO+0.3	V	-
Output low level	VOL	IOL = 16.2 mA	-		0.35	V	-
Output high level	VOH	IOH = -16.2 mA	1.95		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.7 SDRAM DDR2 Interface 1.8V DC Electrical Specifications

Table 32: SDRAM DDR2 Interface 1.8V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL	-	-0.3		VREF - 0.125	V	-
Input high level	VIH	-	VREF + 0.125		VDDIO + 0.3	V	-
Output low level	VOL	IOL = 13.4 mA			0.28	V	-
Output high level	VOH	IOH = -13.4 mA	1.42			V	-
Rtt effective impedance value	RTT	See note 2	120	150	180	ohm	1 , 2
			60	75	90	ohm	1 , 2
			40	50	60	ohm	1 , 2
Deviation of VM with respect to VDDQ/2	dVm	See note 3	-6		6	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply VREF +/- 0.25 to input pin separately,
   then measure current $I_{(VREF\ +0.25)}$ and $I_{(VREF\ -0.25)}$ respectively.

$$RTT = \frac{0.5}{I_{(VREF\ +0.25)} - I_{(VREF\ -0.25)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1 \right) \times 100\,\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.8 PCI Interface 3.3V DC Electrical Specifications

Table 33: PCI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.5*VDDIO		VIO+0.5	V	-
Output low level	VOL	IOL = 1.5 mA	-		0.1*VDDIO	V	-
Output high level	VOH	IOH = -0.5 mA	0.9*VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

6.5.9 UART Interface 3.3V DC Electrical Specifications

Table 34: UART Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.10 Device Bus 3.3V DC Electrical Specifications

Table 35: Device Bus 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.11 Two-Wire Serial Interface (TWSI) 3.3V DC Electrical Specifications

Table 36: TWSI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.5.12 JTAG Interface 3.3V DC Electrical Specifications

Table 37: JTAG Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	2.4		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

General comment: See the Pin Description section for internal pullup/pulldown.

1. While I/O is in High-Z.

2. This current does not include the current flowing through the pullup/pulldown resistor.

6.6 AC Electrical Specifications

See Section 6.7, Differential Interface Electrical Characteristics, on page 80 for differential interface specifications.

6.6.1 Reference Clock AC Timing Specifications

Table 38: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Core Reference Clock					
Frequency	$F_{CORE\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{CORE\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{CORE\_REF\_CLK}$		200	ps	
Slew rate	$SR_{CORE\_REF\_CLK}$	0.7		V/ns	1
CORE_REF_CLK Spread Spectrum Requirements					
Frequency Modulation	$Fmod_{CORE\_REF\_CLK}$	0	33	kHz	
F Spread	$Fspread_{CORE\_REF\_CLK}$	-1	0	%	
CPU Reference Clock					
Frequency	$F_{CPU\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{CPU\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{CPU\_REF\_CLK}$		200	ps	
Slew rate	$SR_{CPU\_REF\_CLK}$	0.7		V/ns	1
CPU_REF_CLK Spread Spectrum Requirements					
Frequency Modulation	$Fmod_{CPU\_REF\_CLK}$	0	33	kHz	
F Spread	$Fspread_{CPU\_REF\_CLK}$	-1	0	%	
SATA and USB Reference Clock					
Frequency	$F_{SATA\_USB\_REF\_CLK}$	25 - 100 ppm	25 + 100 ppm	MHz	
Clock duty cycle	$DC_{SATA\_USB\_REF\_CLK}$	40	60	%	
Clock peak-to-peak jitter	$JITP2P_{SATA\_USB\_REF\_CLK}$		200	ps	
Slew rate	$SR_{SATA\_USB\_REF\_CLK}$	0.7		V/ns	1
Ethernet Reference Clocks					
Frequency in RGMII mode	$F_{RGE\_CLK\_125}$	125 - 50 ppm	125 + 50 ppm	MHz	

Table 38: Reference Clock AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Frequency in GMII mode	$F_{GGE\_CLK\_125}$	125 - 100 ppm	125 + 100 ppm	MHz	
Frequency in MII 100 Mbps mode	F_{GE_RXCLK} F_{GE_TXCLK}	25 - 100 ppm	25 + 100 ppm	MHz	
Frequency in MII 10 Mbps mode	F_{GE_RXCLK} F_{GE_TXCLK}	2.5 - 100 ppm	2.5 + 100 ppm	MHz	
Frequency in MMII mode	F_{GE_RXCLK} F_{GE_TXCLK}	50 - 100 ppm	50 + 100 ppm	MHz	
RGMII/GMII clock duty cycle	$DC_{GE\_CLK\_125}$	45	55	%	
MII clock duty cycle	DC_{GE_TXCLK} DC_{GE_RXCLK}	35	65	%	
Slew rate	$SR_{GE\_REF\_CLK}$	0.7		V/ns	1
SMI Master Mode Reference Clock					
SMI output MDC clock	F_{GE_MDC}	Core-Clock/128		MHz	
TWSI Master Mode Reference Clock					
SCK output clock	F_{TWSI_SCK}	Core-Clock/1600		kHz	
PCI Out Clock					
Frequency	F_{PCLK}		33/66	MHz	3
TCLK_OUT Out Clock					
Frequency	F_{TCLK_OUT}		166	MHz	
Clock duty cycle	DC_{TCLK_OUT}	40	60	%	2

Notes:

1. Slew rate is measured from 20% to 80% of the reference clock signal.
2. The load is CL = 15 pF.
3. The maximum is either 33 MHz or 66 MHz (see PCI_M66EN in Table 21, PCI Reset Configuration, on page 44).
   The PCI Out Clock is relevant when the MPP[21:20] is configured as PCI Out Clock (see DEV_D[14] in Table 20, Reset Configuration, on page 41).
   For PCI Out Clock timing and waveforms, refer to Section 6.6.7, PCI Interface AC Timing, on page 72.

Figure 5: TCLK Out Reference Clock Test Circuit

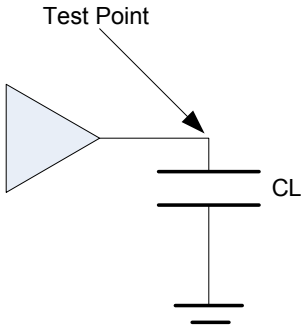
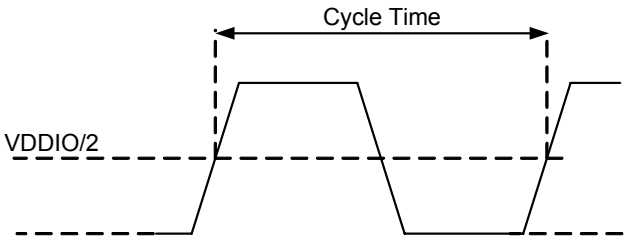


Figure 6: TCLK Out AC Timing Diagram



6.6.2 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

6.6.2.1 RGMII AC Timing Table

Table 39: RGMII- ID (PHY Internal Delay) AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	125.00		MHz	-
Data to Clock output skew (at transmitter)	TskewT	-0.50	0.50	ns	2
Data to Clock input setup (at receiver –integrated delay)	TsetupR	1.00	-	ns	-
Data to Clock input hold (at receiver –integrated delay)	TholdR	1.00	-	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

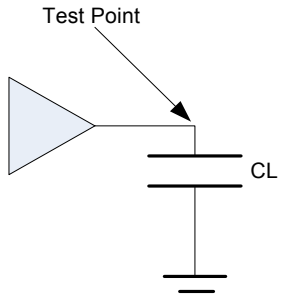
General comment: tCK = 1/fCK.

1. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns respectively.

2. For all signals the load is CL = 5 pF.

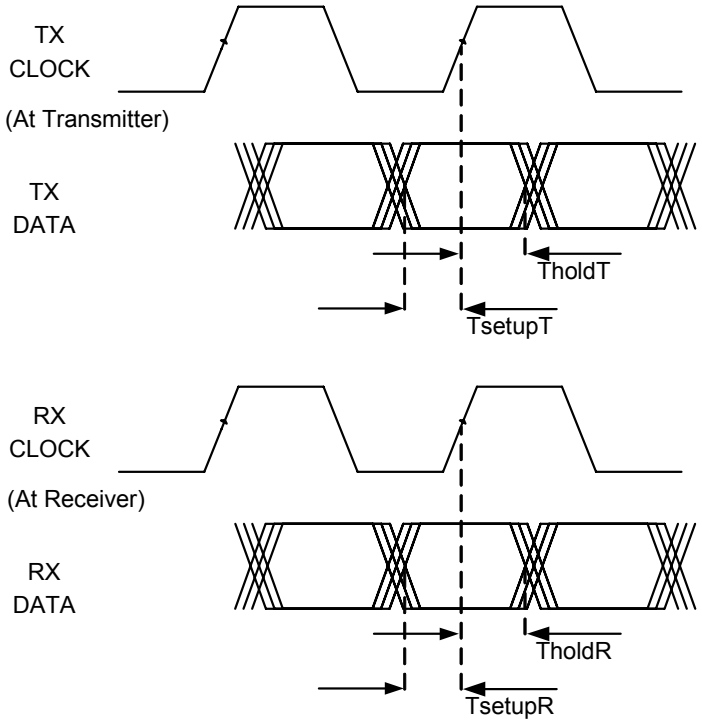
6.6.2.2 RGMII Test Circuit

Figure 7: RGMII Test Circuit



6.6.2.3 RGMII AC Timing Diagram

Figure 8: RGMII-ID (PHY Internal Delay) AC Timing Diagram



6.6.3 Gigabit Media Independent Interface (GMII) AC Timing

In this section, the signal names GTX_CLK and RX_CLK are referred to as GE_TXCLK and GE_RXCLK respectively, in the 88F5182.

6.6.3.1 GMII AC Timing Table

Table 40: GMII AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
GTX_CLK cycle time	tCK	7.5	8.5	ns	-
RX_CLK cycle time	tCKrx	7.5	-	ns	-
GTX_CLK and RX_CLK high level width	tHIGH	2.5	-	ns	1
GTX_CLK and RX_CLK low level width	tLOW	2.5	-	ns	1
GTX_CLK and RX_CLK rise time	tR	-	1.0	ns	1, 2
GTX_CLK and RX_CLK fall time	tF	-	1.0	ns	1, 2
Data input setup time relative to RX_CLK rising edge	tSETUP	2.0	-	ns	-
Data input hold time relative to RX_CLK rising edge	tHOLD	0.0	-	ns	-
Data output valid before GTX_CLK rising edge	tOVB	2.5	-	ns	1
Data output valid after GTX_CLK rising edge	tOVA	0.5	-	ns	1

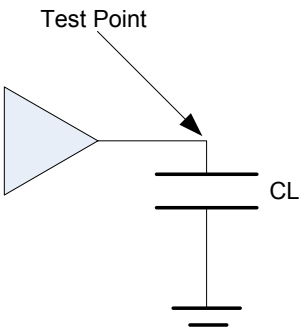
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

6.6.3.2 GMII Test Circuit

Figure 9: GMII Test Circuit



6.6.3.3 GMII AC Timing Diagrams

Figure 10: GMII Output Delay AC Timing Diagram

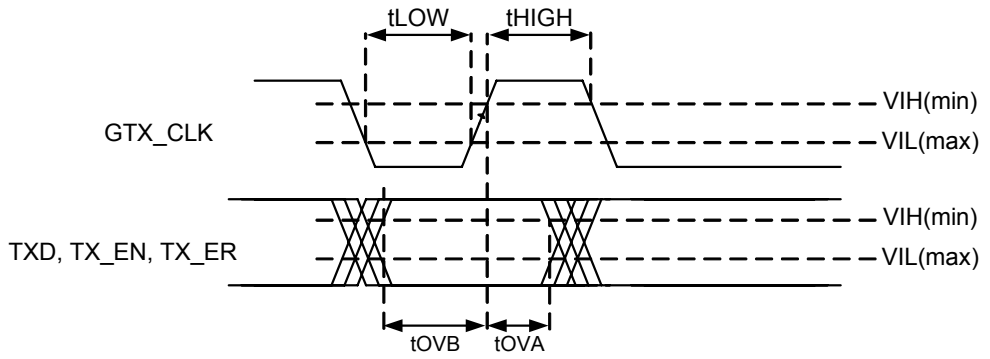
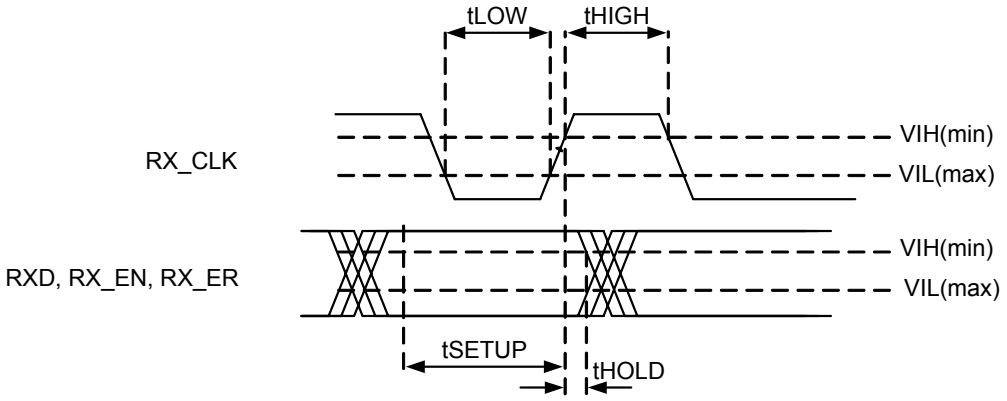


Figure 11: GMII Input AC Timing Diagram



6.6.4 Media Independent Interface (MII/MMII) AC Timing

6.6.4.1 MII/MMII AC Timing Table

Table 41: MII/MMII AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

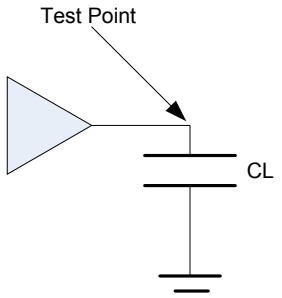
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

6.6.4.2 MII/MMII Test Circuit

Figure 12: MII/MMII Test Circuit



6.6.4.3 MII/MMII AC Timing Diagrams

Figure 13: MII/MMII Output Delay AC Timing Diagram

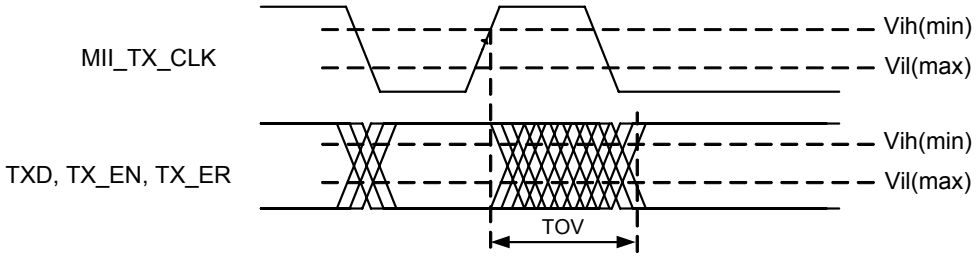
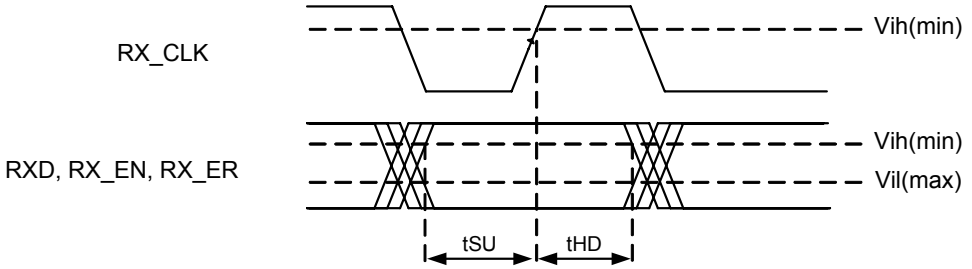


Figure 14: MII/MMII Input AC Timing Diagram



6.6.5 Serial Management Interface (SMI) AC Timing

In this section, the signal names MDC and MDIO are referred to as GE_MDC and GE_MDIO respectively, in the 88F5182.

6.6.5.1 SMI AC Timing Table

Table 42: SMI AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	40.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	-
MDIO output valid before MDC rise time	tOVB	15.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	15.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For MDC signal, the load is CL = 390 pF, and for MDIO signal, the load is CL = 470 pF.

2. See "Reference Clocks" table for more details.

6.6.5.2 SMI Test Circuit

Figure 15: MDIO Test Circuit

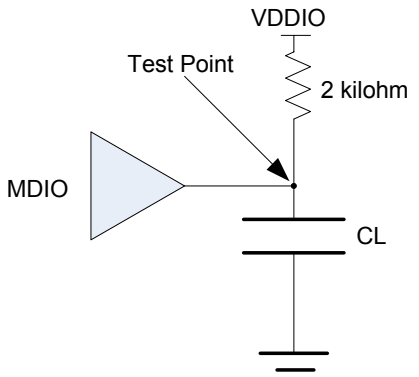
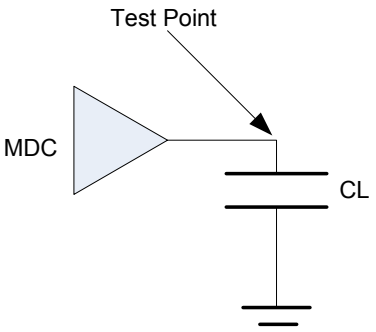


Figure 16: MDC Test Circuit



6.6.5.3 SMI AC Timing Diagrams

Figure 17: SMI Output Delay AC Timing Diagram

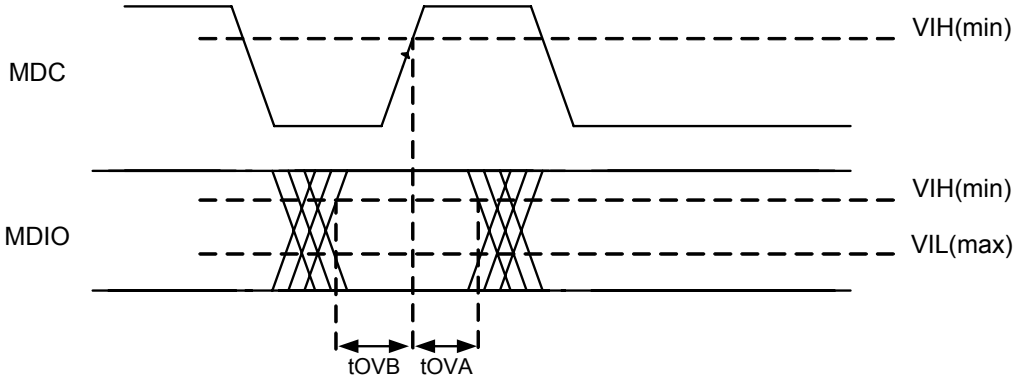
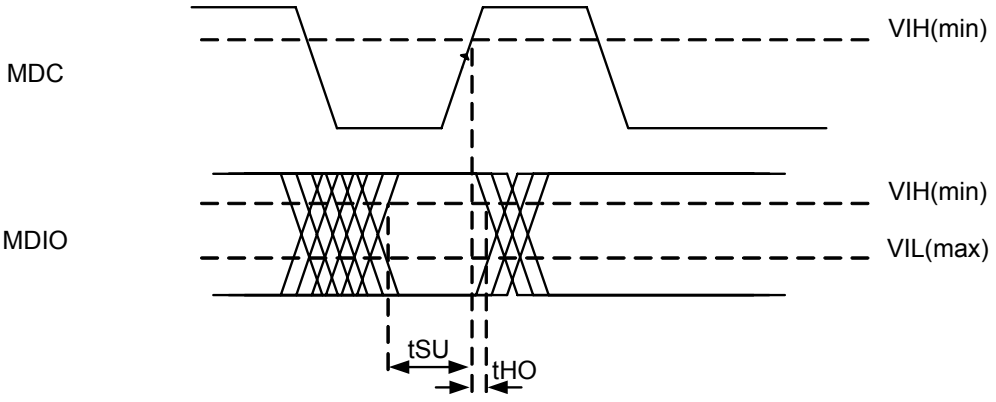


Figure 18: SMI Input AC Timing Diagram



6.6.6 SDRAM DDR2 Interface AC Timing

6.6.6.1 SDRAM DDR2 Interface AC Timing Table

Table 43: SDRAM DDR2 Interface AC Timing Table

Description	Symbol	200 MHz @ 1.8V		Units	Notes
		Min	Max		
Clock frequency	fCK	200.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	0.50	-	ns	-
DQ and DM valid output time after DQS transition	tDOVA	0.50	-	ns	-
DQ and DM output pulse width	tDIPW	0.35	-	tCK	-
DQS output high pulse width	tDQSH	0.35	-	tCK	-
DQS output low pulse width	tDQSL	0.35	-	tCK	-
DQS falling edge to CLK-CLKn rising edge	tDSS	0.34	-	tCK	1
DQS falling edge from CLK-CLKn rising edge	tDSH	0.34	-	tCK	1
CLK-CLKn rising edge to DQS output rising edge	tDQSS	-0.11	0.11	tCK	-
DQS write preamble	tWPRE	0.35	-	tCK	-
DQS write postamble	tWPST	0.41	-	tCK	-
CLK-CLKn high-level width	tCH	0.45	0.55	tCK	1
CLK-CLKn low-level width	tCL	0.45	0.55	tCK	1
DQ input setup time relative to DQS in transition	tDSI	-0.55	-	ns	-
DQ input hold time relative to DQS in transition	tDHI	1.50	-	ns	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	2.25	-	ns	1, 2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	0.70	-	ns	1, 2
Address and control output pulse width	tIPW	0.67	-	tCK	-

Notes:

General comment: All timing values were measured from vref to vref, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate measured from Vref +/-125 mV).

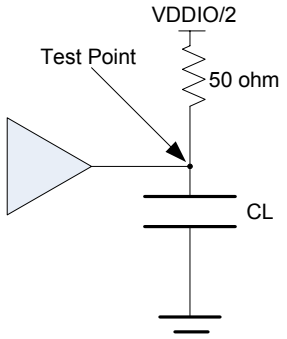
General comment: tCK = 1/fCK.

General comment: For all signals, the load is CL = 16 pF.

1. This timing value is defined on CLK / CLKn crossing point.
2. This timing value is defined when Address and Control signals are output ¼tCK after CLK-CLKn rising edge.
   For more information, see register settings.

6.6.6.2 SDRAM DDR2 Interface Test Circuit

Figure 19: SDRAM DDR2 Interface Test Circuit



6.6.6.3 SDRAM DDR2 Interface AC Timing Diagrams

Figure 20: SDRAM DDR2 Interface Write AC Timing Diagram

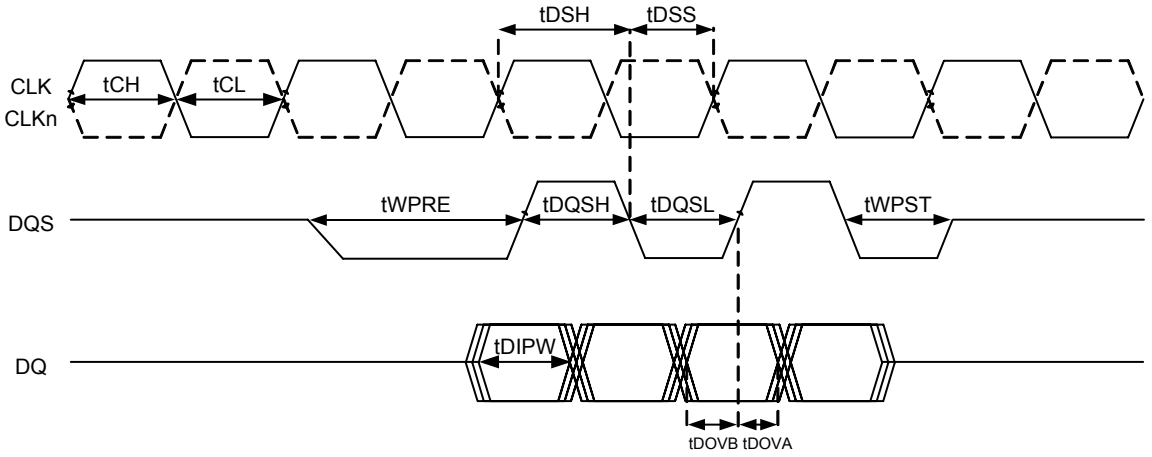


Figure 21: SDRAM DDR2 Interface Address and Control AC Timing Diagram

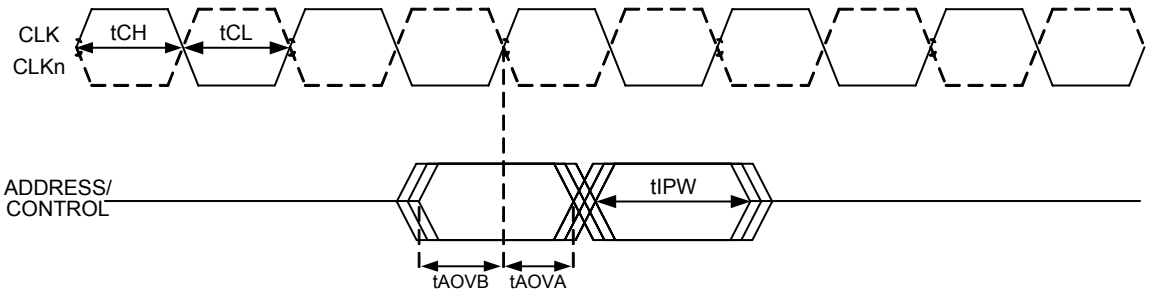
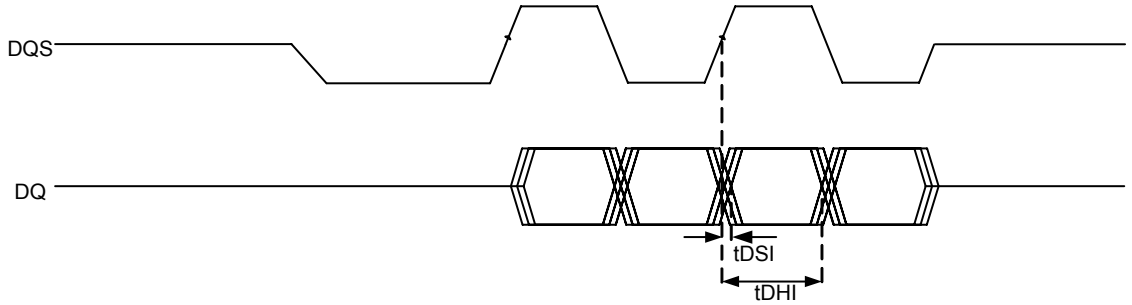


Figure 22: SDRAM DDR2 Interface Read AC Timing Diagram



6.6.7 PCI Interface AC Timing

6.6.7.1 PCI Interface AC Timing Table

Table 44: PCI Interface AC Timing Table

Description	Symbol	PCI 66 MHz @ 3.3V		PCI 33 MHz @ 3.3V		Units	Notes
		Min	Max	Min	Max		
Clock cycle time	Tcyc	15.0	30.0	30.0	-	ns	1
Clock high time	Thigh	6.0	-	11.0	-	ns	-
Clock low time	Tlow	6.0	-	11.0	-	ns	-
Clock slew rate	-	1.5	4.0	1.0	4.0	V/ns	2
Clock rising edge to signal valid delay for bused signals	Tval	2.0	6.0	2.0	11.0	ns	3, 4
Clock rising edge to signal valid delay for point to point signals	Tval(ptp)	2.0	6.0	2.0	12.0	ns	3, 4
Input setup time to Clock rising edge for bused signals	Tsu	3.0	-	7.0	-	ns	4, 6, 8
Input setup time to Clock rising edge for point to point signals	Tsu(ptp)	5.0	-	10, 12	-	ns	4, 5, 6
Input hold time from Clock rising edge	Th	0.0	-	0.0	-	ns	6
Reset active time	Trst	1.0	-	1.0	-	ms	7
Output rise slew rate	tr	1.0	4.0	1.0	4.0	V/ns	9
Output fall slew rate	tf	1.0	4.0	1.0	4.0	V/ns	9

Notes:
1. The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.
2. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in the PCI Interface Clock waveform.
3. See the timing measurment conditions in the Output Timing Measurement Conditions figure.
4. Point-to-point signals applies to REQn and GNTn only. All other signals are bused.
5. For PCI 33 MHz: GNTn has a setup of 10 ns; REQn has a setup of 12 ns.
6. See the timing measurement conditions in the Input Timing Measurement Conditions figure.
7. RSTn is asserted and deasserted asynchronously with respect to Clock.
8. Setup time applies only when the device is not driving the pin.
   Devices cannot drive and receive signals at the same time.
9. The test load is specified in the Tval (Min) Test Load figure.

6.6.7.2 PCI Clock Spread Spectrum Requirements Table

Table 45: PCI Clock Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	30.0	33.0	kHz	-
Fspread	-1.0	0.0	%	-

General comment: Relevant for Conventional PCI 66 MHz only.

6.6.7.3 PCI Interface Test Circuit

Figure 23: Tval (Max) Rising Edge Test Load

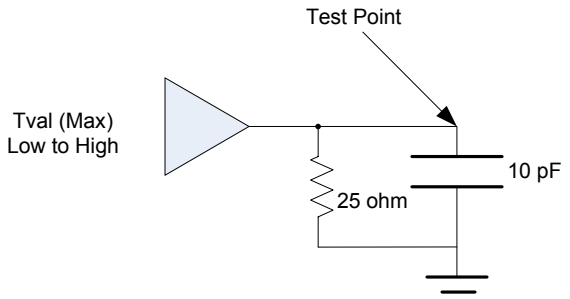


Figure 24: Tval (Max) Falling Edge Test Load

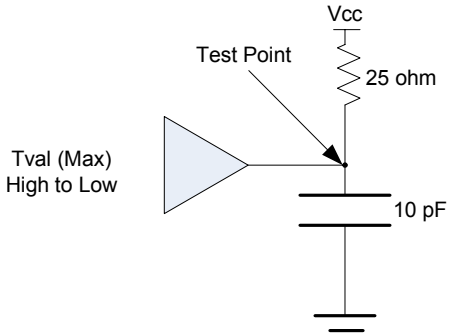
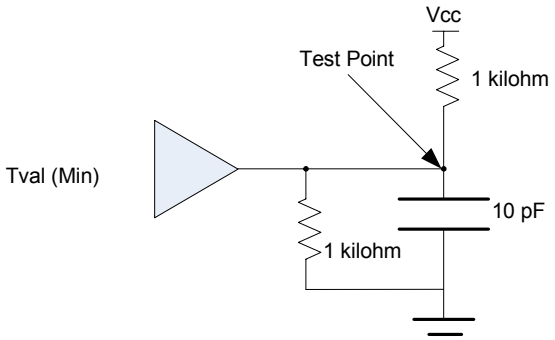


Figure 25: Tval (Min) Test Load & Output Slew Rate Test Load



6.6.7.4 PCI Interface Measurement Condition Parameters

Table 46: PCI Interface Measurement Condition Parameters

Symbol	PCI	Units	Notes
Vth	0.6 Vcc	V	-
Vtl	0.2 Vcc	V	-
Vtest	0.4 Vcc	V	-
Vtrise	0.285 Vcc	V	1
Vtfall	0.615 Vcc	V	1
Output rise slew rate	0.3 Vcc to 0.6 Vcc	V	-
Output fall slew rate	0.6 Vcc to 0.3 Vcc	V	-
Input signal slew rate	1.5	V/ns	-

Notes:
1. Vtrise and Vtfall are reference voltages for timing definitions only.

6.6.7.5 PCI Interface AC Timing Measurement Waveforms

Figure 26: PCI Interface Clock Waveform

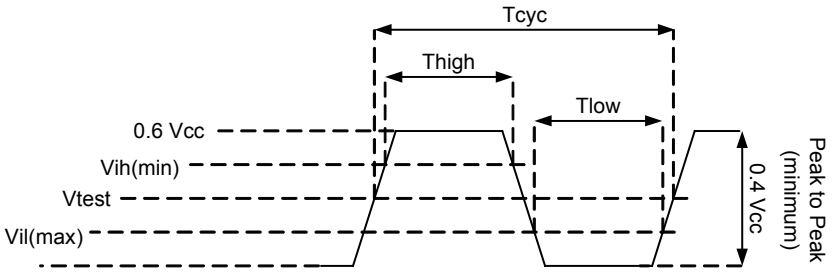


Figure 27: PCI Interface Output Timing Measurement Conditions

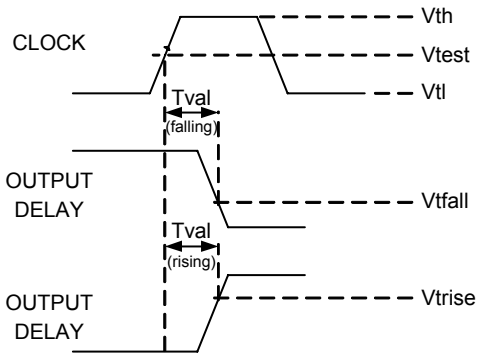
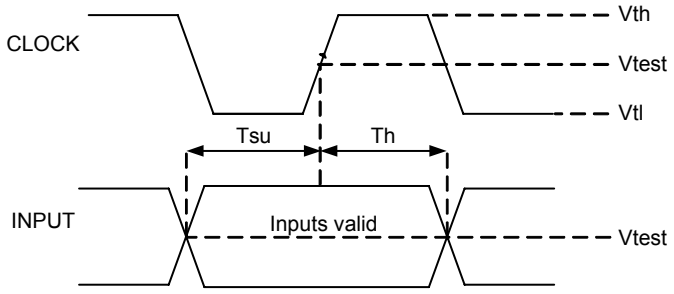


Figure 28: PCI Interface Input Timing Measurement Conditions



6.6.8 Two-Wire Serial Interface (TWSI) AC Timing

6.6.8.1 TWSI AC Timing Table

Table 47: TWSI AC Timing Table

Description	Symbol	100 kHz		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

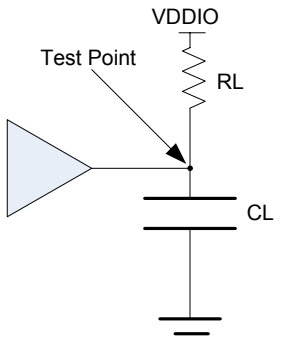
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

6.6.8.2 TWSI Test Circuit

Figure 29: TWSI Test Circuit



6.6.8.3 TWSI AC Timing Diagrams

Figure 30: TWSI Output Delay AC Timing Diagram

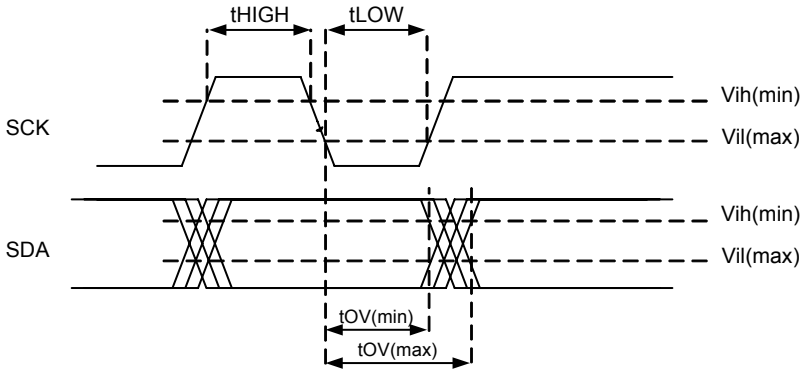
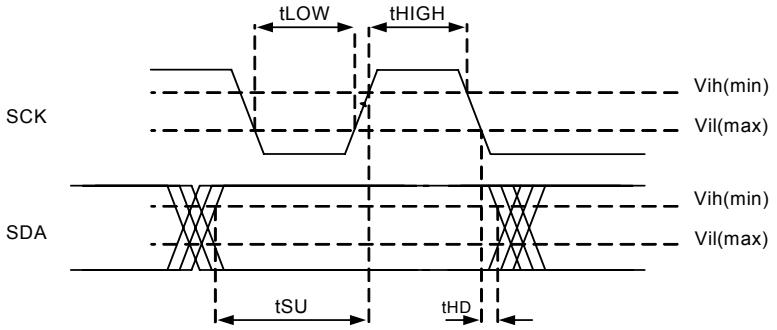


Figure 31: TWSI Input AC Timing Diagram



6.6.9 JTAG Interface AC Timing

6.6.9.1 JTAG Interface AC Timing Table

Table 48: JTAG Interface AC Timing Table

Description	Symbol	5 MHz		Units	Notes
		Min	Max		
JTClk frequency	fCK	5.0		MHz	-
JTClk minimum pulse width	Tpw	0.40	0.60	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.50	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	10.0	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	75.0	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	20.0	ns	1

Notes:

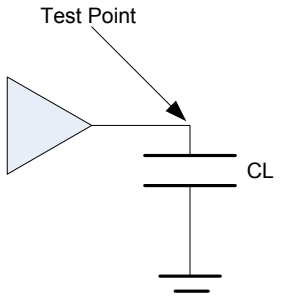
General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 20 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.

6.6.9.2 JTAG Interface Test Circuit

Figure 32: JTAG Interface Test Circuit



6.6.9.3 JTAG Interface AC Timing Diagrams

Figure 33: JTAG Interface Output Delay AC Timing Diagram

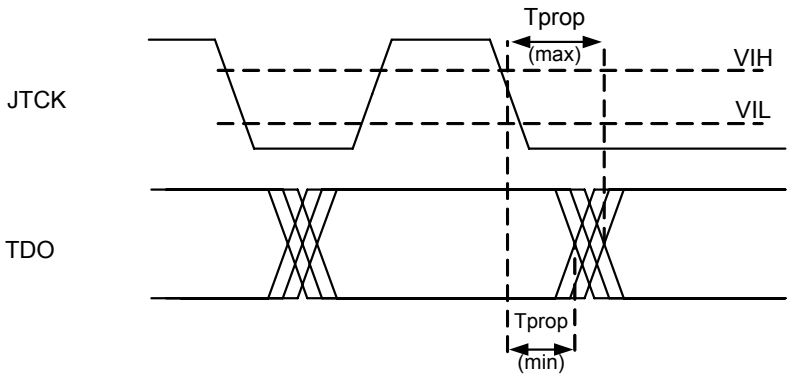
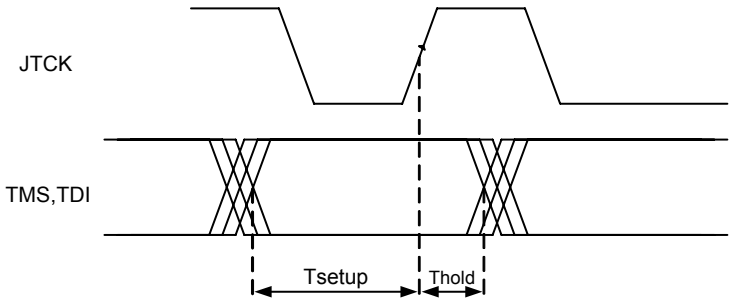


Figure 34: JTAG Interface Input AC Timing Diagram



6.7 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express (PEX) Interface Electrical Characteristics
- SATA Interface Electrical Characteristics
- USB Interface Electrical Characteristics

6.7.1 Differential Interface Reference Clock Characteristics

6.7.1.1 PCI Express Interface Differential Reference Clock Characteristics

Table 49: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Input Clock frequency	fCK	100.0		MHz	-
Input Clock duty cycle	DCrefclk	0.45	0.55	tCK	-
Input Clock rise/fall time	TRrefclk	175.0	700.0	pS	1, 3
Input Clock rise/fall time variation	dlTRrefclk	-	125.0	pS	1, 3
Input high voltage	VIHrefclk	660.0	850.0	mV	1
Input low voltage	VILrefclk	-150.0	50.0	mV	1
Absolute crossing point voltage	Vcross	250.0	550.0	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140.0	mV	1
Absolute maximum input voltage (overshoot)	Vmax	-	1.15	V	1
Absolute minimum input voltage (undershoot)	Vmin	-	-0.3	V	1
Absolute differential clock period	Tperabs	9.872	-	nS	2
Differential clock cycle-to-cycle jitter	Tccjit	-	125.0	pS	-

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 1.0a, April 2003, section 2.6.3 for more information.

1. Defined on a single ended signal.
2. Including jitter and spread spectrum.
3. Defined from 0.175V to 0.525V.

6.7.2 PCI Express (PEX) Interface Electrical Characteristics

6.7.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 50: PCI Express Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400.0		ps	-
Baud rate tolerance	Bppm	-300.0	300.0	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.7	-	UI	-
Differential return loss	TRLdiff	12.0	-	dB	1
Common mode return loss	TRLcm	6.0	-	dB	1
DC differential TX impedance	ZTXdiff	80.0	120.0	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	15.0	-	dB	1
Common mode return loss	RRLcm	6.0	-	dB	1
DC differential RX impedance	ZRXdiff	80.0	120.0	Ohm	-
DC common input impedance	ZRXcm	40.0	60.0	Ohm	-

Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.0a, April, 2003.

1. Defined from 50 MHz to 1.25 GHz.
2. Does not account for SSC dictated variations.

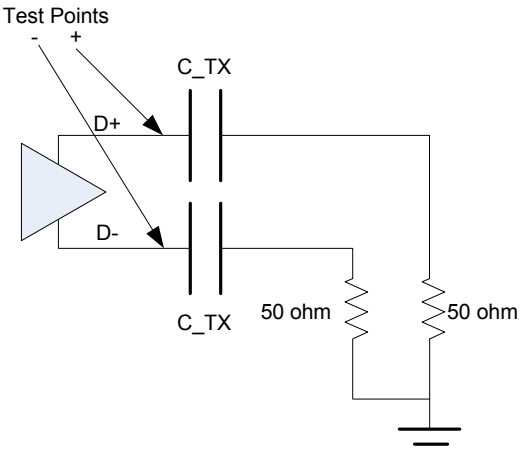
6.7.2.2 PCI Express Interface Spread Spectrum Requirements

Table 51: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	30.0	33.0	kHz	-
Fspread	-0.5	0.0	%	-

6.7.2.3 PCI Express Interface Test Circuit

Figure 35: PCI Express Interface Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

6.7.3 SATA Interface Electrical Characteristics

6.7.3.1 SATA-I Interface Gen1i Mode Driver and Receiver Characteristics

Table 52: SATA-I Interface Gen1i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	-
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Input differential voltage	Vdiffrx	325.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	-
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	-

Notes:

General Comment: For more information, refer to SATA II Phase 1.0 Specification, August, 2004.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.

6.7.3.2 SATA-II Interface Gen2i Mode Driver and Receiver Characteristics

Table 53: SATA-II Interface Gen2i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLOD	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.30	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.17	UI	3
Total jitter at connector clock-data	TJ500	-	0.37	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.19	UI	4
Receiver Parameters					
Input differential voltage	Vdiffrx	275.0	750.0	mV	5
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLID	1.0	-	dB	-
Total jitter at connector clock-data	TJ10	-	0.46	UI	3
Deterministic jitter at connector clock-data	DJ10	-	0.35	UI	3
Total jitter at connector clock-data	TJ500	-	0.60	UI	4
Deterministic jitter at connector clock-data	DJ500	-	0.42	UI	4

Notes:

General Comment: For more information, refer to SATA II Phase 1.0 Specification, August, 2004.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See functional register description for more details.
3. Defined for BR/10.
4. Defined for BR/500.
5. 0.5 UI is the point where the signal meets the minimum level.

6.7.4 USB Interface Electrical Characteristics

6.7.4.1 USB Driver and Receiver Characteristics

Table 54: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 55: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1.. Defined with 1.425 kilohm pull-up resistor to 3.6V.

2.. Defined with 14.25 kilohm pull-down resistor to ground.

3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.

4. See "Data Signal Rise and Fall Time" waveform.

5. Including frequency tolerance. Timing difference between the differential data signals.

6. Defined at crossover point of differential data signals.

Table 56: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

6.7.4.2 USB Interface Driver Waveforms

Figure 36: Low/Full Speed Data Signal Rise and Fall Time

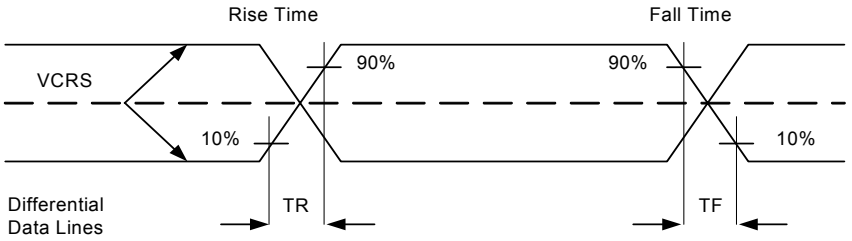


Figure 37: High Speed TX Eye Diagram Pattern Template

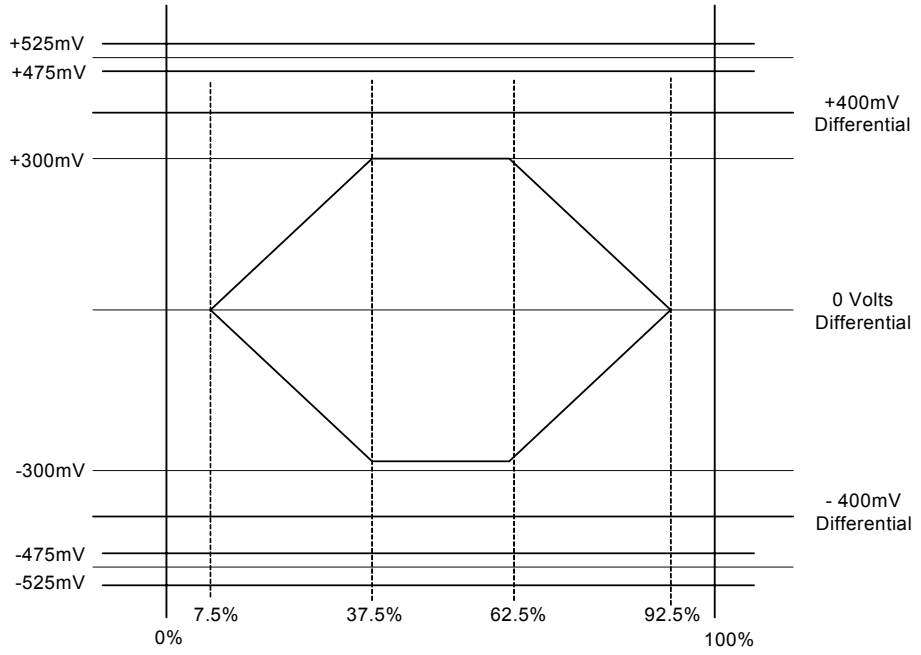
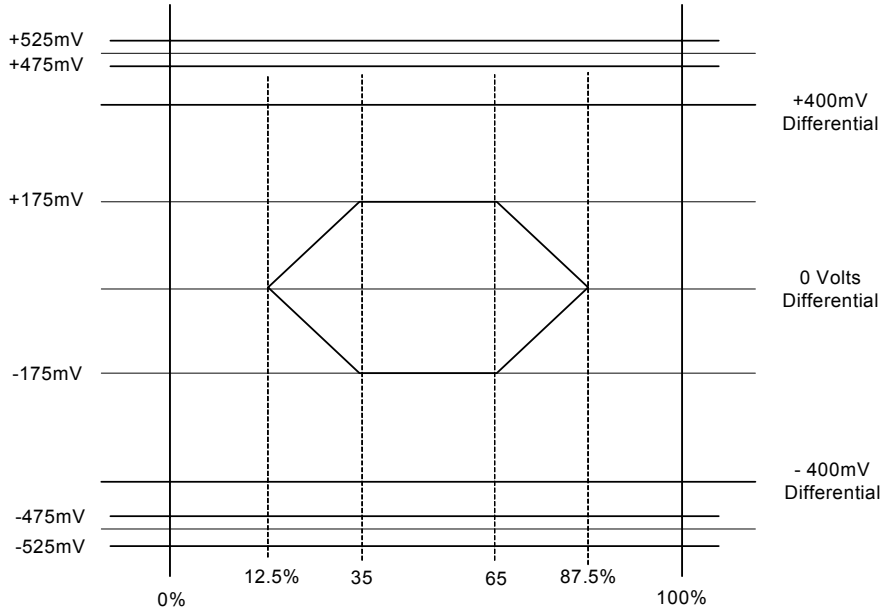


Figure 38: High Speed RX Eye Diagram Pattern Template



7 Thermal Data

Note

It is recommended to read application note AN-63 Thermal Management for Selected Marvell® Products (Document Number MV-S300281-00) and the ThetaJC, ThetaJA, and Temperature Calculations White Paper, available from Marvell, before designing a system. These documents describe basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 57 provides the thermal data for the 88F5182. The simulation was done according to JEDEC standards.

Table 57: Package Thermal Data

Parameter	Definition	Airflow Value		
		0 m/s	1 m/s	2 m/s
θ_{JA}	Thermal resistance: junction to ambient	15.5 C/W	13.6 C/W	12.8 C/W
Ψ_{Jt}	Thermal characterization parameter: junction to top center	2.9 C/W		
θ_{JC}	Thermal resistance: junction to case	4.2 C/W		
Ψ_{JB}	Thermal characterization parameter: junction to the bottom of the package.	7.3 C/W	7.1 C/W	7.0 C/W
θ_{JB}	Thermal resistance: junction to the bottom of the package (not air-flow dependent)	8.0 C/W		

8 Package Mechanical Dimensions

The 88F5182 uses a 388-pin Heat Slug Ball Grid Array (HSBGA) 23 x 23 mm package.

Figure 39: 388-pin HSBGA (23 x 23 mm) Package Diagram

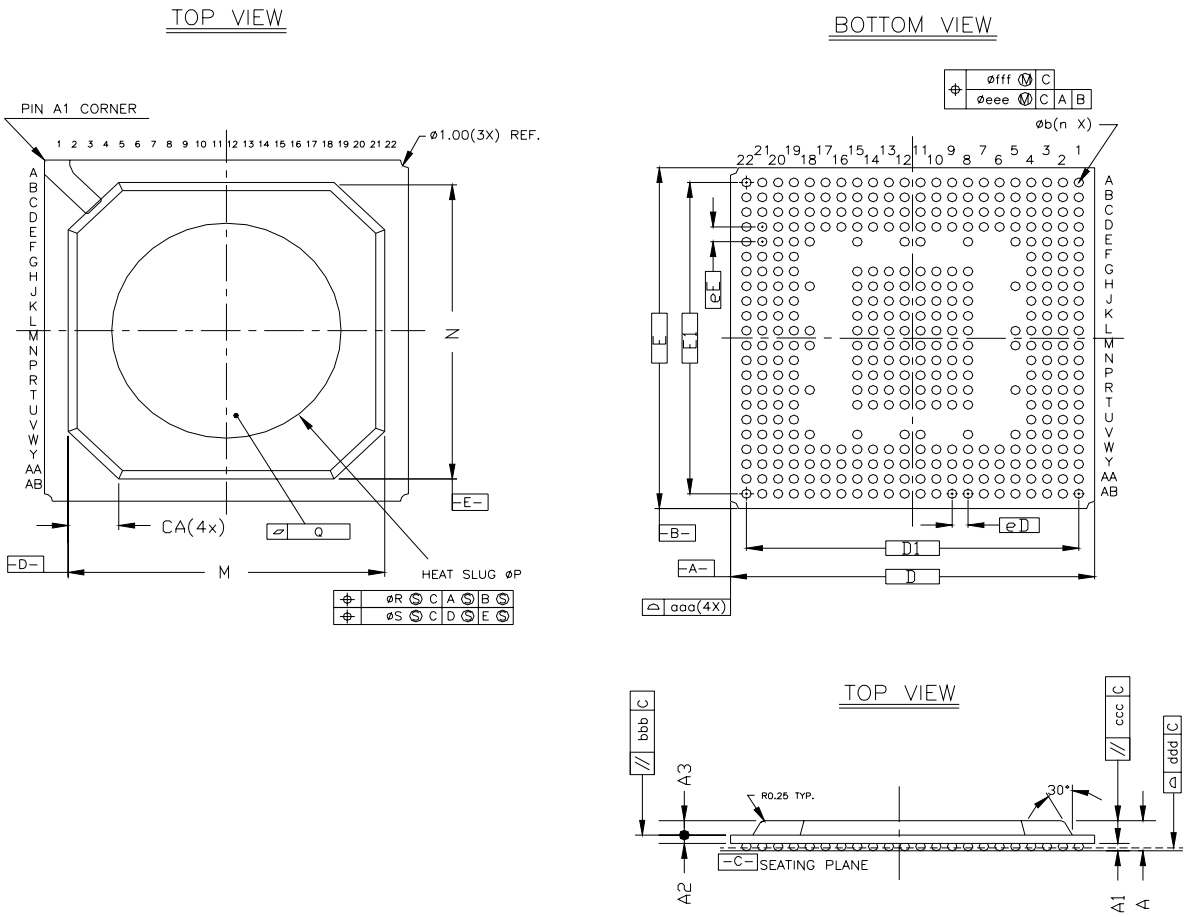


Table 58: 388 HSBGA Package Dimensions

Ball Pitch: 1.0	Substrate Thickness: 0.56
Ball Diameter: 0.6	Mold Thickness: 1.22

Table 59: Package Drawing Key

		Symbol	Common Dimensions
Package :			HS BGA
Body Size:	X	D	23
	Y	E	23
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	2.030 ±0.130
Mold Thickness :		A3	0.970 Ref.
Substrate Thickness :		A2	0.560 Ref.
Ball Diameter :			0.600
Stand Off :		A1	0.400 ~ 0.600
Ball Width :		b	0.500 ~ 0.700
Mold Area :	X	M	20.000
	Y	N	20.000
H/S Exposed Size :		P	14.500 ~ 15.500
H/S Coplanarity :		Q	0.100
H/S Shift With Substrate Edge :		R	0.300
H/S Shift With Mold Area :		S	0.500
Chamfer		CA	3.200 REF.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.200
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	388
Edge Ball Center to Center :	X	D1	21.000
	Y	E1	21.000

9 Part Order Numbering/Package Marking

Figure 40 is an example of the part order numbering scheme for the 88F5182.

Figure 40: Sample Part Number

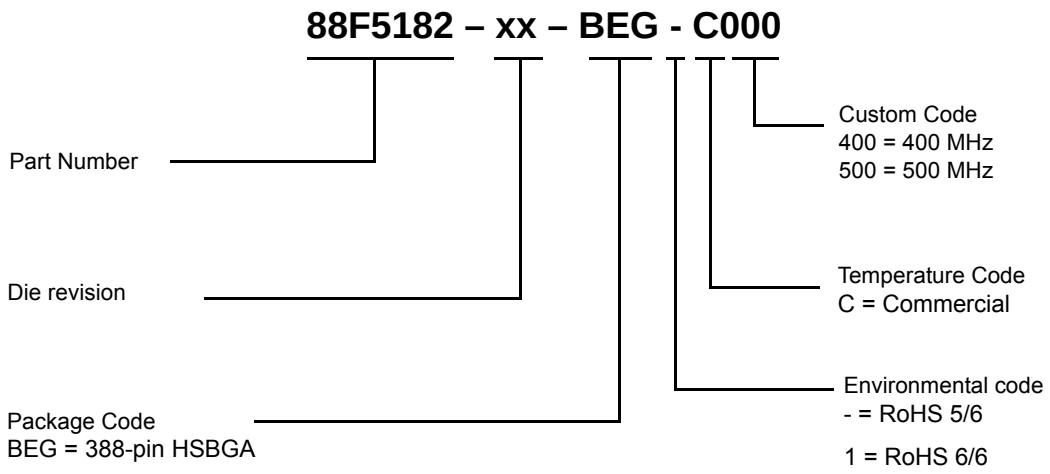
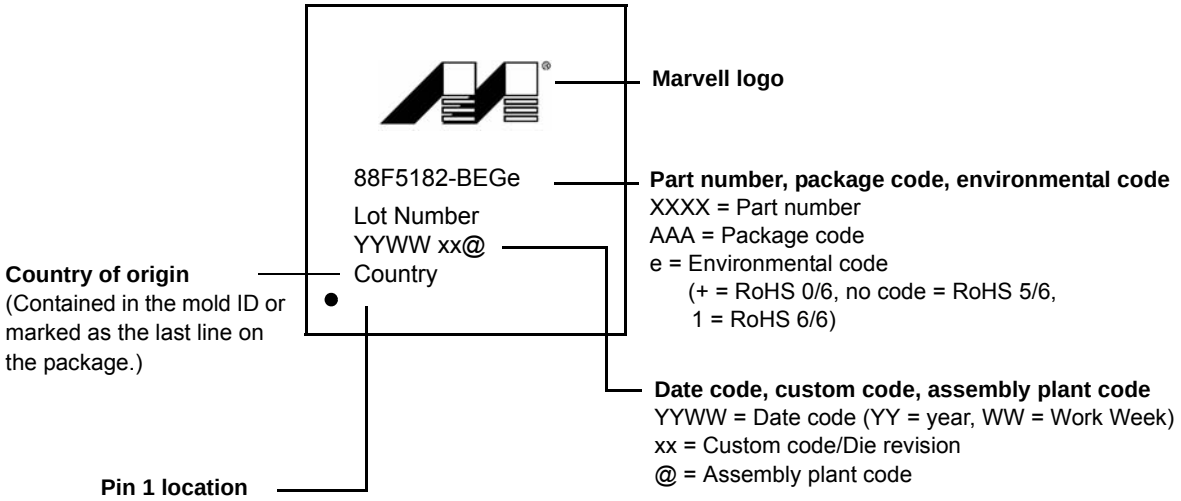


Table 60: 88F5182 Part Order Options

Package Type	Part Order Number
HSBGA (23x23 mm, 388-pin package) 400 MHz	88F5182-xx-BEG-C400 (RoHS 5/6 compliant package)
HSBGA (23x23 mm, 388-pin package) 400 MHz	88F5182-xx-BEG1C400 (RoHS 6/6 compliant package)
HSBGA (23x23 mm, 388-pin package) 500 MHz	88F5182-xx-BEG-C500 (RoHS 5/6 compliant package)
HSBGA (23x23 mm, 388-pin package) 500 MHz	88F5182-xx-BEG1C500 (RoHS 6/6 compliant package)

Figure 41 shows a sample package marking and pin 1 location of the 88F5182.

Figure 41: 88F5182 Package Marking and Pin 1 Location



NOTE: The above example is not drawn to scale. The location of markings is approximate.

A Revision History

Table 61: Revision History

Document Type	Revision	Date
Initial Release	A	September 18, 2005
First Revision	B	October 16, 2005
1. Revised Figure 2, 88F5182 Pinout Map (Top View Left Side), on page 30, Figure 3, 88F5182 Pinout Map (Top View Right Side), on page 31, and Table 15, 88F5182 Pin List, on page 32 to change: ■ Pin U1 to USB_DP[1] ■ Pin U2 to USB_DM[1] ■ The row designation from row Z to row Y. 2. In Section 5.1, Hardware Reset, on page 38, added pins MPP[21:20] to the list. 3. In Table 20, Reset Configuration, on page 41, in the row DEV_ALE[0], revised the note to *Must be pulled to 1*. 4. In Table 23, “Recommended Operating Conditions,” on page 51, added the rows CPU PLL quiet power supply and Core PLL quiet power supply.		
Release	C	March 22, 2006
1. In the Features list, added Proprietary 200 Mbps Marvell MII (MMII) interface on page 4. 2. In 1 "Pin Information" on page 14, added additional pin type and power rail information. 3. In Table 1.2.5, Gigabit Ethernet Port Interface Pin Assignments, on page 23, revised the description of GE_TXCLK to indicate that the clock operates at 2.5 MHz, 25 MHz, or 50 MHz. Also made the same change for the MII Receive Clock description under the GE_RXCLK. pin. 4. Added Section 1.3, Internal Pull-up and Pull-down Pins List, on page 31. 5. In Section 5.5, Pins Sample Configuration, on page 41, updated internal pull up/down resistor to 150 kilohm, and added note to DEV_A[1:0] “When the reference clock is not in use, it must be connected to VSS.” 6. Extensive changes in 6 "Electrical Specifications (Preliminary)" on page 46. 7. In Section 6.2, Recommended Operating Conditions, on page 48, VDD_CPU can now operate at 1.2V as well as 1.4V, and T_AVVD can now operate at 2.5V as well as 3.3V. 8. Changed format of Section Table 24:, Thermal Power Dissipation, on page 49 and Section Table 25:, Current Consumption, on page 50. 9. Added MII, MMII and SMI to Section 6.6.1, Reference Clock AC Timing Specifications, on page 58. 10. Revised the tOV, tSU, and tHD timing values in Table 41, MII/MMII AC Timing Table, on page 65. 11. Split tOV parameter and value changed from 20 to 15 in Table 42, SMI AC Timing Table, on page 67 and in Figure 17, SMI Output Delay AC Timing Diagram, on page 68. 12. In Table 1, SDRAM DDR1 32-bit Interface AC Timing Table, on page 2: • Added General comment: All input timing values assume minimum slew rate of 1V/ns • Changed tDQSS parameter minimum requirement to 0.75 tCK, and tDSI parameter minimum requirement to 0.50 ns • Changed tDSS and tDSH parameters minimum requirement to 0.34 tC. 13. In Table 43, SDRAM DDR2 Interface AC Timing Table, on page 69: • Added General comment: All input timing values assume minimum slew rate of 1V/ns • Changed tDSS and tDSH parameters from 0.24 to 0.34 tCK • Added tDSS/tDSH reference to note #1. 14. Added new note “GNTn has a setup of 10ns; REQn has a setup of 12ns” in Table 44, PCI Interface AC Timing Table, on page 72		
15. Added Table 45, PCI Clock Spread Spectrum Requirements, on page 72.		

Table 61: Revision History (Continued)

Document Type	Revision	Date
16. Changed Table 48, JTAG Interface AC Timing Table, on page 78 from 10 to 5 MHz.		
Release	D	January 22, 2008
1. In Table 1, 88F5182 Interface Pin Logic Diagram, on page 14 and Table 6, SATA II Interface Pin Assignment, on page 22 changed the SATA_RES pin to output. 2. In Table 2, 88F5182 Pin Map and Pin List, on page 32, the pinout and pin list are inserted as an Excel file attachment. 3. In Table 12, Device Bus Interface Pin Assignments, on page 28, changed description of DEV_WEn[1:0] to Device Bus Byte Write Enable and added multiplexed pins information. 4. In Table 20, Reset Configuration, on page 41, changed Note for Dev_D[14] to internally pulled down to 0. 5. In Table 38, Reference Clock AC Timing Specifications, on page 58, changed value of SCK output clock from core clock/3200 to core clock/1600 and added MII clock duty cycle. 6. Revised Section 6.7, Differential Interface Electrical Characteristics, on page 80. Added Section 6.7.2, PCI Express (PEX) Interface Electrical Characteristics, on page 81, Section 6.7.3, SATA Interface Electrical Characteristics, on page 83 and Section 6.7.4, USB Interface Electrical Characteristics, on page 85. 7. Added Table 59, Package Drawing Key, on page 91. 8. Updated Figure 41, 88F5182 Package Marking and Pin 1 Location, on page 93.		
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